# Semiconductor Device Manufacturing & Inspection Equipment

## 1 Trends in Advanced Semiconductor Devices and Customer Requirements for Manufacturing and Inspection Equipment

As payments and other applications for processing information using smartphones become more widespread and the Internet of Things (IoT) continues to grow, the amount of data being generated and processed is expanding dramatically. Meanwhile, the spread of 5th-generation (5G) telecommunications and the rollout of autonomous driving are expected to increase the quantity of this data even further. As advanced logic and memory devices are used to process this huge amount of data and utilize it for prediction and decision making, demand for these advanced devices is predicted to grow.

In logic devices and in dynamic random-access memory (DRAM), further miniaturization of device size continues along with the structural transition [from fin field effect transistors (FinFETs) to gate-all-around (GAA) transistors in logic devices]. As for three-dimensional (3D-) NAND flash memory in which memory cells are vertically stacked, higher bit density is achieved by increasing the number of stacked layers. Devices with 96 layers are already in production and those with more than 200 layers are in the pipeline. In the development and manufacturing of these advanced semiconductor devices, technologies that can fabricate these complex structures with high precision are required as well as the inspection and measurement technologies for controlling these processes. The inspection of the backside of wafers is also necessary because backside control is important for manufacturing these advanced devices with high yield.

Hitachi will continue to supply technologies and solutions to meet these diverse customer requirements.
(Hitachi High-Tech Corporation)

Semiconductor logic devices

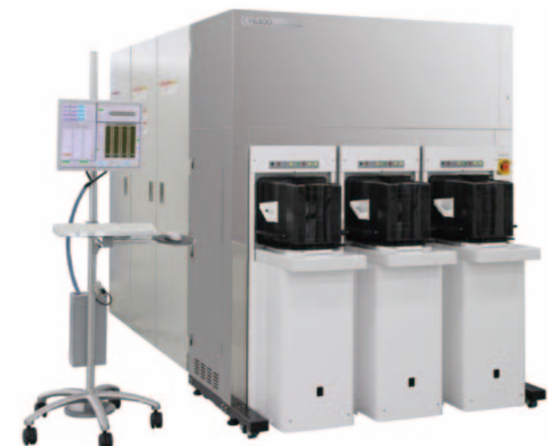
| Year | 2018 | 2019 | 2020 | 2021 | 2022 | … | 2025 |
|---|---|---|---|---|---|---|---|
| Technology node (nm) | 10 to 7 | | 7 to 5 | | 5 to 3 | | 3 to 2.1 |
| Gate pitch (nm) | 54 | | 48 | | 45 | | 42 |
| Wiring pitch (nm) | 36 | | 30 | | 24 | | 21 |
| Transistor structure | | | FinFET (Gate, n, p, fin) | | | | GAAFET (n, p, Gate, Nano-Sheet) |

Memory devices

| Year | 2018 | 2019 | 2020 | 2021 | 2022 | … | 2025 |
|---|---|---|---|---|---|---|---|
| DRAM technology node (nm) | up to 18 | | up to 17 | up to 16 | < up to 15 | | |
| No. of 3D-NAND layers | 64 to 72 | up to 96 | | up to 128 | > more than 200 | | |

Source: Estimated by Hitachi High-Tech Corporation based on IRDS2018.

**1** Advances in latest logic and memory devices



**2** CV6300 series high-voltage CD-SEM for measurement of deep hole and trench bottom dimensions and precise overlay measurement

## 2 High-voltage CD-SEM for Measurement of Deep Hole and Trench Bottom Dimensions and Precise Overlay Measurement

Along with miniaturization, the latest 3D-NAND flash memory also achieves higher levels of integration through the stacking of memory cells, with 96-layer stacking currently possible. The simultaneous measurement of both the top-most and bottom-most pattern layers, for which a greater depth of processing is required due to stacking, enables highly accurate process management by predicting the performance of the resulting devices.

The CV6300 series of high-voltage critical dimension scanning electron microscopes (CD-SEMs) are the first in-line dimensional measurement system in the world* to use an acceleration voltage of 45 kV, achieving precise measurement of deep hole and trench bottom dimensions by enhancing image quality using the electrons reflected from the bottom-most layers. The series also delivers throughput that is approximately 25% higher than the previous model thanks to features such as a new wafer stage, with improved adjustment precision and stability of the primary electron beam to enhance precision and reduce variability among measurement systems in the overlay measurement function as well as dimensional measurement. In their use as process control systems, not only for memory devices, but also for the production of other semiconductor integrated circuits where growing use is being made of 3D structures, the CV6300 series is able to satisfy diverse customer needs.
(Hitachi High-Tech Corporation)

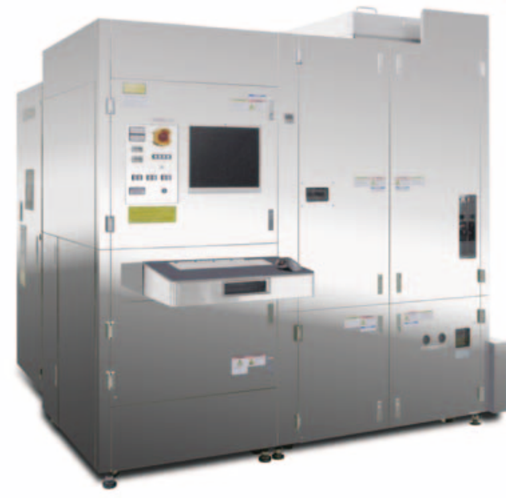
* Based on research by High-Tech Corporation

## 3 Wafer Surface Inspection System for Front- and Back-side Inspection with High Speed and Sensitivity

Wafer surface inspection systems for inspecting semiconductor wafers prior to forming the circuit pattern are widely used in various semiconductor device production processes, including shipping inspection and quality checks on incoming wafers, and to control cleanliness and sustain the quality of manufacturing equipment. Furthermore, in order to maintain and manage the yield of leading-edge semiconductor devices, there is also strong demand for the ability to inspect the back as well as the front side of the wafer with high sensitivity and throughput.

To satisfy these requirements, Hitachi High-Tech has launched the LS9300A-EG wafer surface inspection system for front- and back-side inspection with high sensitivity and throughput. The system features an edge grip (EG) function that grips wafers by their edges to perform inspections without applying suction to the back of the wafer or compromising back side cleanliness, and also a wafer flipping mechanism that allows inspection of the back side of the wafer also.

The LS9300A-EG is also suited to a wider range of applications, including inspecting both sides of wafers with high sensitivity and throughput during inward and outward goods inspection, and the rapid detection of defects caused by factors such as the presence of impurities on the back side of the wafer.
(Hitachi High-Tech Corporation)



**3** LS9300A-EG wafer surface inspection system for front- and back-side inspection with high sensitivity and throughput