Semiconductor Manufacturing and Inspection Technologies for the 0.1 μm Process Generation

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OVERVIEW: In the 0.1 μm process generation, we are progressing toward what is being called the "system on a chip." The promotion of that trend requires more than the LSI technology for increasing the integration scale of CMOS (complementary metal-oxide semiconductor) devices as suggested in the ITRS (International Technology Roadmap for Semiconductors). Also required is progress in the development of new materials for finer patterning and core integration technology through intimate cooperation of technologies for design, device/process, and manufacturing and inspection equipment. That will make it possible to provide the customer with the best solution from among diverse goals and approaches. The 0.1 μm-generation LSI chips feature high integration scale, with CMOS gate lengths of 0.1 μm or less, the integration of DRAM (dynamic random access memory), flash memory, BiCMOS (bipolar CMOS), analog cores, etc., and eight or nine layers of multi-layer wiring. Another feature is the full use of new materials, of which high-κ (dielectric constant) gate insulation films, copper wiring and low-κ interlayer films are typical. Such issues in LSI fabrication and inspection technology can be classified into those related to processes for (1) larger integration scale, (2) use of new materials, (3) core mixing and those related to production technology for (4) shorter development turnaround time (TAT) and (5) lower cost.

INTRODUCTION

OVER the past 30 years, progress in semiconductor manufacturing technology has centered on technology for increasing the scale of integration, and inspection technology has also strengthened in correspondence with the higher integration scales. For MOS (metal-oxide semiconductor) devices in particular, polycrystalline silicon gate process technology and ion implantation doping technology has basically taken over MOS structure since their establishment in 1970.

Prior to the 0.1 μm process generation, progress was basically a matter of increasingly finer CMOS (complementary MOS) structures[1]. Realizing that, however, involved issues of gate insulation layer technology, technology for source, drain and channel formation, contact formation technology, multi-layer wiring technology and so on in addition to finer process technology.

Those issues involve the physical limits of device structures and materials and so required more than simply higher precision in manufacturing technology; they required a reconsideration of materials and a new control parameter, stress.

When CMOS devices are employed as a platform for the integration of various types of devices such as DRAM (dynamic random access memory), flash memory, BiCMOS (bipolar CMOS), and analog cores, issues arise that are peculiar to the integration of these devices and that do not relate to the individual core processes (see Fig. 1).

Furthermore, in order to achieve shorter turnaround time (TAT) for LSI development while maintaining yield and reliability, inspection and analysis technology for analyzing device structures and materials on the atomic or molecular level and the construction of a system that makes use of information technology (IT) for systematic feedback of that knowledge to manufacturing are important.

Here, we describe the semiconductor fabrication and inspection technology of the 0.1 μm era.

Business Goal	Supply electronic components		Supply solution		
Customer	Partners		Partners		
Product	Components CMOS LSI products		Best solution System LSI products		
LSI technology	Common goal (ITRS)		Diverse goals and approaches		
			Core integration technology for system solution		
	Faster, cheaper, shorter-TAT CMOS LSIs		Faster, lower power, cheaper, and shorter-TAT CMOS LSI		
			DRAM core / Flash memory core / BiCMOS core / Analog core / New core		
	Higher integration scale for CMOS devices		Higher integration scale and new materials for the CMOS platform		
Basic technology	Design / Device/process / Manufacturing and inspection		Design ↔ Device/process ↔ Manufacturing and inspection		

CMOS : complementary metal-oxide semiconductor
ITRS : International Technology Roadmap for Semiconductors
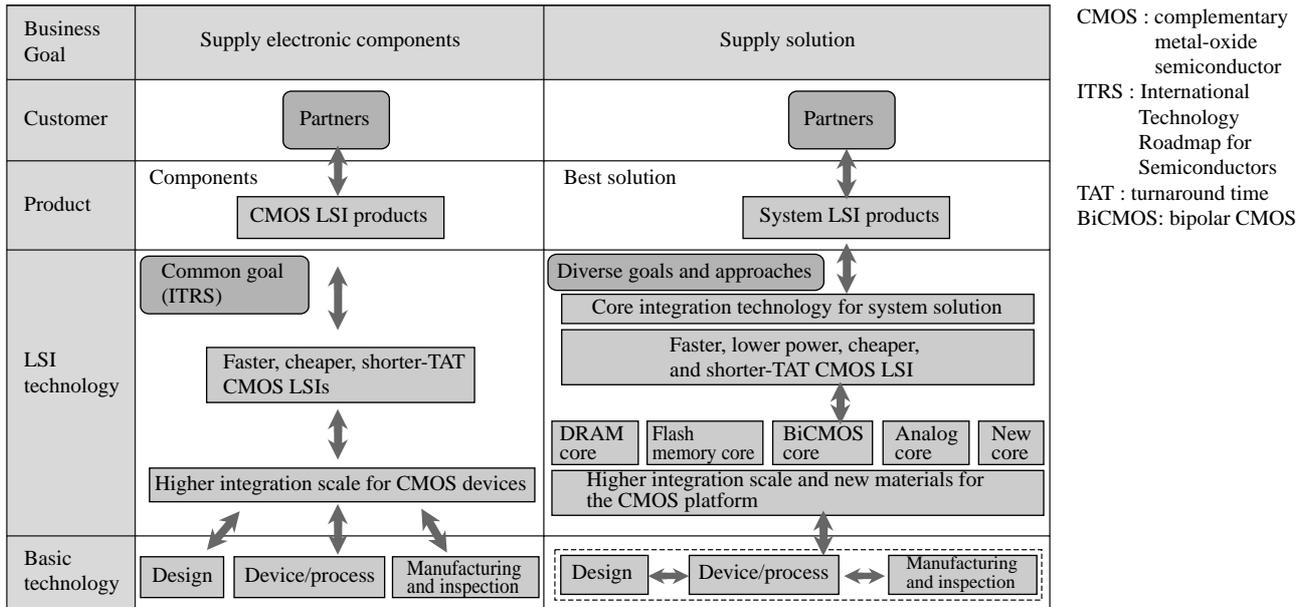TAT : turnaround time
BiCMOS: bipolar CMOS

Fig. 1—System LSI That Supports the Best Solution.
In the 'system on a chip' era, it is important to provide the customer with the system LSI that is the best solution selected from among diverse goals and approaches through intimate coordination of the various technologies for design, device/processes, and manufacturing and inspection.

DEVICE PROCESS TECHNOLOGY
Higher Integration Scale for CMOS Devices

CMOS devices are switches that turn the current flow between source and drain on and off by controlling the formation of an electrically conductive layer (channel). When the voltage above the threshold is applied to the gate electrode, the electrical potential of the silicon surface below the gate changes, forming the channel. The basic performance of this switch is determined by how large a drive current flows when the switch is on and how small the leak current is when the switch is turned off.

The most effective ways to obtain a large drive current in the on state, are to reduce the gate length and use a thin-film gate insulation layer. Respectively, these methods increase the drive current by shortening the distance that the carriers travel in the channel and increasing the number of carriers. It is also known that the carrier mobility changes greatly with the stress that is applied to the channel[2], so it is important for stress design to begin in the device design stage.
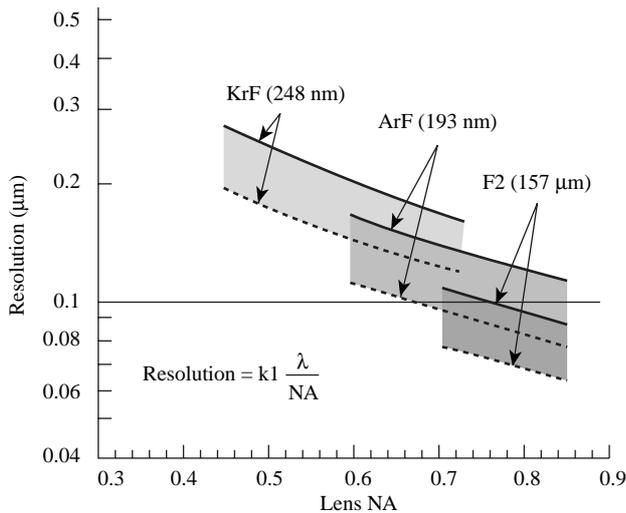
Because the drive current greatly depends on the gate length in this way, there are strict precision requirements for the gate electrode fabrication processes in particular, including a dimensional deviation of 10% or less and vertical wall shapes. The shape requirement results from the fact that ion implantation is performed with highly precise angle control using the gate electrode as a mask.

At the center of the technologies for fine fabrication processes are lithography technology and dry etching technology. In lithography, higher resolution is achieved by using light sources that have shorter wavelengths for the stepper and lenses that have higher NA (numerical aperture) values (Fig. 2). To achieve dimensional resolutions of 0.1 μm or less, it is essential to change the light source wavelength from 248 nm (KrF) to 193 nm (ArF) and to have an NA of at least 0.7. Together with those conditions, has come the need for development of a resist for use with ArF. In addition, dimension resolution that is finer than the light wavelength has become possible by making full use of the resolution enhancement technology known as phase shifting and modified illumination[3].

To cope with the increasingly severe process requirements for gate length accuracy, there is a need for design automation technology that can compensate for process fluctuations beginning at the pattern design stage. It is necessary to further advance OPC (optical proximity correction) technology and to perform comprehensive compensation that takes into account the amount of dry etching dimension shifting as well as the light intensity distribution in lithography.

In dry etching technology, accurate resist

Fig. 2—Relationships Among Resolution of Stepper Technology, Lens Numeric Aperture, and Light Wavelength.
Shorter stepper light source wavelength and higher NA increase resolution.

$$\text{Resolution} = k1\ \frac{\lambda}{NA}$$

——— : k1 = 0.50 when resolution enhancement is not used
- - - - - : k1= 0.35 when resolution enhancement is used
k1: process coefficient   NA: numerical aperture   λ: wavelength
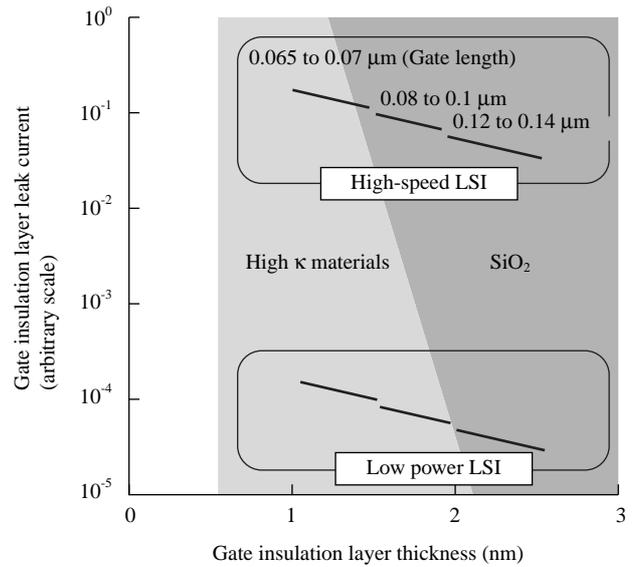

Fig. 3—Relation Between Gate Insulation Layer Thickness and Gate Insulation Layer Leak Current.
For a film thickness of 1.5 nm or less for high-speed LSIs and 2 nm or less for low power LSIs, the leak current due to tunneling current cannot be achieved with SiO_2.

dimensions are fundamental. In future, the target gate length will be below the resolution of the stepper, so technology for reducing the resist dimensions will also be required[4]. Also important is prevention of changes in the amount of dimension shifting and shape depending on the variation in pattern density and the type of polycrystalline silicon dopant[5].

As the design rule of devices becomes finer, the effect of the stress that arises in the films that form the devices on device characteristics becomes large. In particular, the stress in the polycrystalline silicon film that forms the gate electrode, the stress in the self-aligning silicide film formed above that film, and the stress in the insulation layer that forms the side walls cannot be ignored. The development of "TCAD (technology CAD)" that integrates device processes

and can predict the effects of film stress on the device prior to test fabrication is desirable.

Use of New Materials

For the 0.1 μm generation CMOS devices, the off-state leak current component for which a countermeasure is most necessary is the tunneling current that flows through the gate insulation layer. The leak current target values for high-speed LSI circuits and low power LSI circuits from the ITRS (International Technology Roadmap for Semiconductors) are presented in Table 1. If the thickness of the silicon oxide film that is used for the gate insulation layer is less than 1.5 nm for the high-speed LSI circuits and less than 2 nm for the low power LSI circuits, the leak current due to tunneling current

TABLE 1. Target Values for Gate Insulation Layer Leak Current According to ITRS
Of the off leak current components, countermeasures are most necessary for the tunneling current that flows through the gate insulation layer.

Year		2001	2002	2003	2004
Source voltage (V)		1.2 to 1.5	Same as left	Same as left	0.9 to 1.2
Gate (μm)		0.10	0.085 to 0.090	0.080	0.070
Gate insulation layer thickness (nm)		1.5 to 1.9	Same as left	Same as left	1.2 to 1.5
High-speed LSI	Gate insulation layer leak current (nA/μm)	8	10	13	16
Low power LSI	Gate insulation layer leak current (nA/μm)	0.008	0.010	0.013	0.016

cannot achieve the target values (Fig. 3). This means that a new material must replace silicon oxide as the insulation film material. To satisfy the target values, the film thickness must be increased by replacing the silicon oxide film with a material that has a higher κ (dielectric constant), thus decreasing the tunneling current. There are many candidates for this new material, including the oxides of Ta, Ti, Al, Zr, and Hf as well as silicate films, but the electrical properties of the interface between the high κ material and the silicon are important as well as high dielectric constant.

In order for the high-speed pulses generated by CMOS devices to propagate through the multi-layer wiring with little delay or waveform distortion, reduction of the wiring resistance and interlayer film capacitance is essential. The use of copper for the wiring material and fluorine-doped silicon oxide for the interlayer film has already begun. A TEM (transmission electron microscope) cross-section view of test-fabricated copper multi-layer wiring that employs these materials is shown in Fig. 4. Wiring layers 1 through 5 have a 0.5 µm pitch and were formed by a "dual damascene" process, in which the wiring and through-holes are processed simultaneously. In future, a transition to a shorter wiring pitch and an insulation layer of even lower permittivity will be necessary[6].

According to the ITRS, improvement in the accuracy of the dual damascene method is essential in order to reduce the copper wiring pitch to 0.32 µm and beyond. Particularly necessary are improvement in dry etching technology and copper CMP (chemical-mechanical polishing) technology, which are the main processing technologies, and the establishment of plating technology for embedding copper. With dry etching technology, wiring and through-holes are processed together at one time, so high dimensional accuracy and selectivity are required. As for copper CMP technology, progress is being made in improving the uniformity of the CMP equipment and the provision of process monitoring, as well as the optimization of slurry and pad materials.

Hitachi and Hitachi Chemicals have jointly developed an abrasive-free slurry for use in copper CMP[7, 8]. That slurry allows highly selective polishing with respect to the foundation film, so that even if over-polishing is done to prevent wiring shorts, it is possible to keep the amount of the copper wiring layer and interlayer film that is removed small (Fig. 5). That makes it possible to achieve stable low wiring resistance. The use of this slurry is also known to
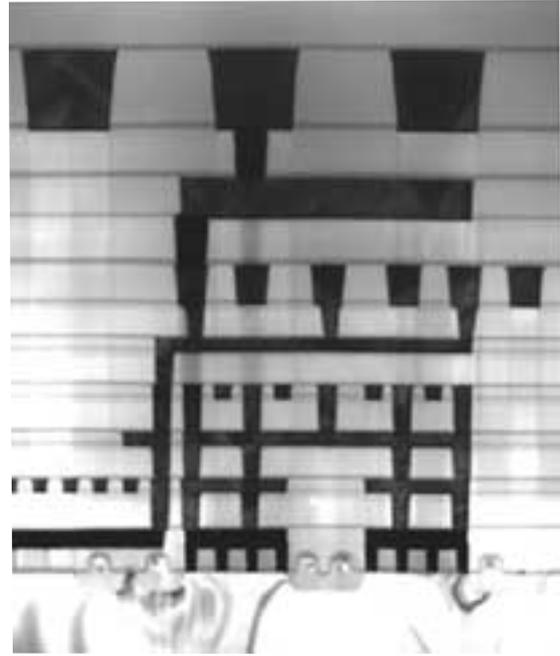

Fig. 4—Cross-section of the Copper Multi-layer Wiring. TEM observation of a cross-section of the copper wiring. The "dual damascene" process was used, in which the wiring and through-holes were formed simultaneously.

reduce surface scratching.

The dielectric constant of the interlayer insulation layer material is reduced from approximately 4.2 for silicon oxide film to approximately 3.7 for fluorine-doped silicon oxide film. In future, films formed by CVD (chemical vapor deposition) or coating will be employed with the objective of reaching a permittivity of 3 or less. The requirements for the interlayer film include, in addition to dielectric constant, (1) no hindrance of copper embedding by out-gassing, (2) high adhesion and barrier characteristics with respect to copper and sufficiently long TDDB (time dependent dielectric breakdown) lifetime, and (3) sufficient mechanical strength to withstand CMP. Currently, CVD film and coated films each have their respective merits and demerits, and their combination is considered to be important.

Core Integration

System LSI chips are beginning to integrate various types of cores, such as DRAM and flash memory, BiCMOS, and analog cores, with CMOS devices serving as the platform. Two integration processes with CMOS are considered, (1) the integration of devices other than CMOS devices and (2) the integration of different types of CMOS devices (Fig. 6).
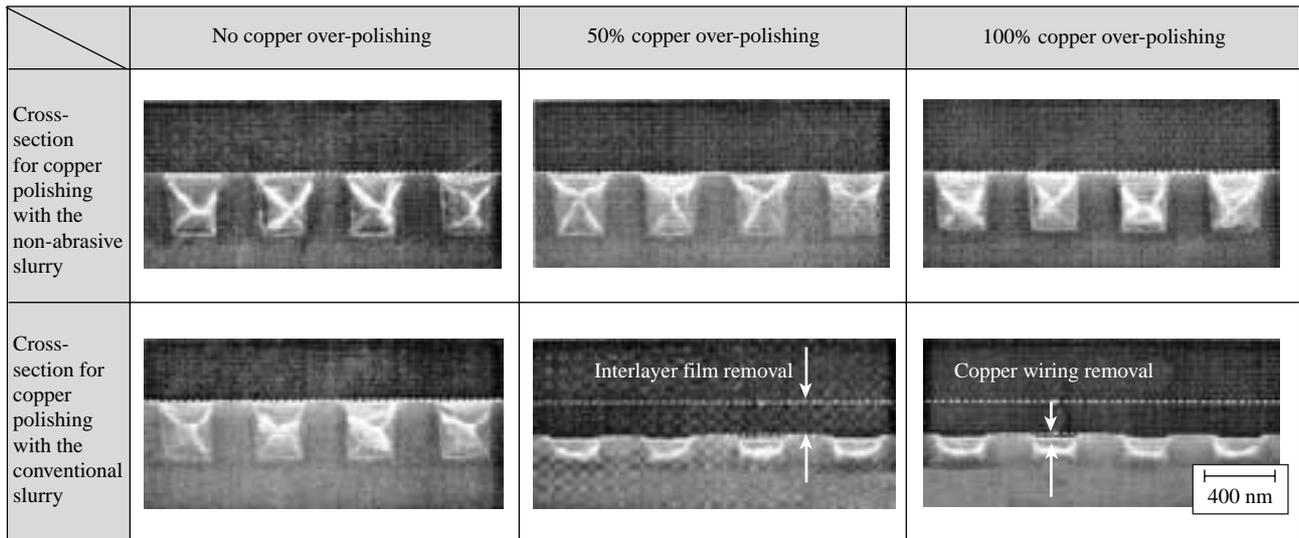
	No copper over-polishing	50% copper over-polishing	100% copper over-polishing
Cross-section for copper polishing with the non-abrasive slurry			
Cross-section for copper polishing with the conventional slurry		Interlayer film removal	Copper wiring removal 400 nm

Fig. 5—Comparison of Cross-sections for When the Copper Polishing Was Done with the Non-abrasive Slurry and with the Conventional Slurry.
When the non-abrasive slurry for copper polishing developed jointly by Hitachi and Hitachi Chemicals was used, polishing that was highly selective with respect to the base film was possible, reducing the removal of the copper wiring layer and the interlayer film.
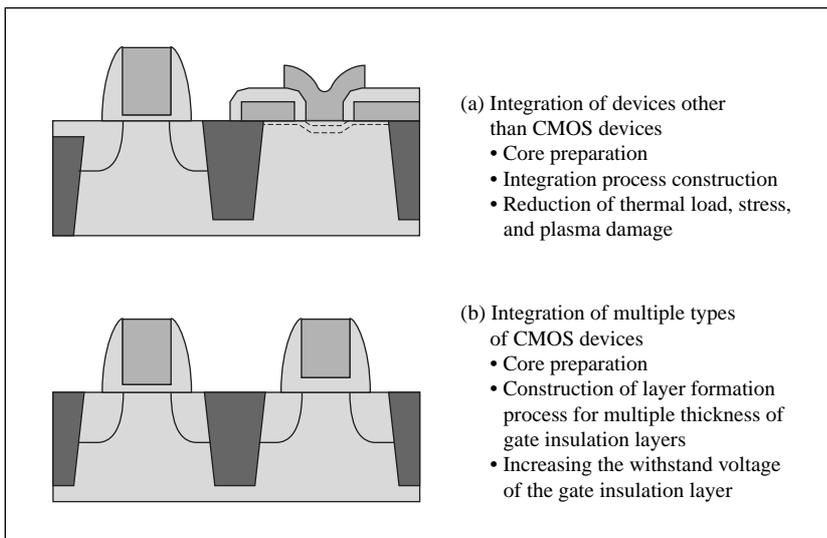
(a) Integration of devices other than CMOS devices
• Core preparation
• Integration process construction
• Reduction of thermal load, stress, and plasma damage

(b) Integration of multiple types of CMOS devices
• Core preparation
• Construction of layer formation process for multiple thickness of gate insulation layers
• Increasing the withstand voltage of the gate insulation layer

Fig. 6—Issues in System LSI Process Construction.
In both (a) and (b), the technology for integrating various cores is modularized, making it possible to integrate any combination of cores immediately.

For case (1), there is likely to be increased thermal load and stress as well as plasma damage, because processes for forming the non-CMOS devices are used in addition to the CMOS processes. Concerning thermal load in particular, it is important to reduce the temperature and the time of thermal treatments in the non-CMOS processes so as to avoid degradation of the CMOS device characteristics.

For case (2), CMOS devices of different source voltages are formed according to the user-specified input-output voltages, which creates the need to make gate insulation films of different thickness. The methods of making gate oxide films of different thicknesses include using a resist process and employing wet etching and ion implantation. In any case, the problem is to preserve the withstand voltage of the gate insulation layer, so optimization of the resist removal and washing method is known to be important.

For both case (1) and case (2), it is necessary to develop the ability to immediately implement the integration of any combination of cores upon request through the modularization of various core integration technologies.
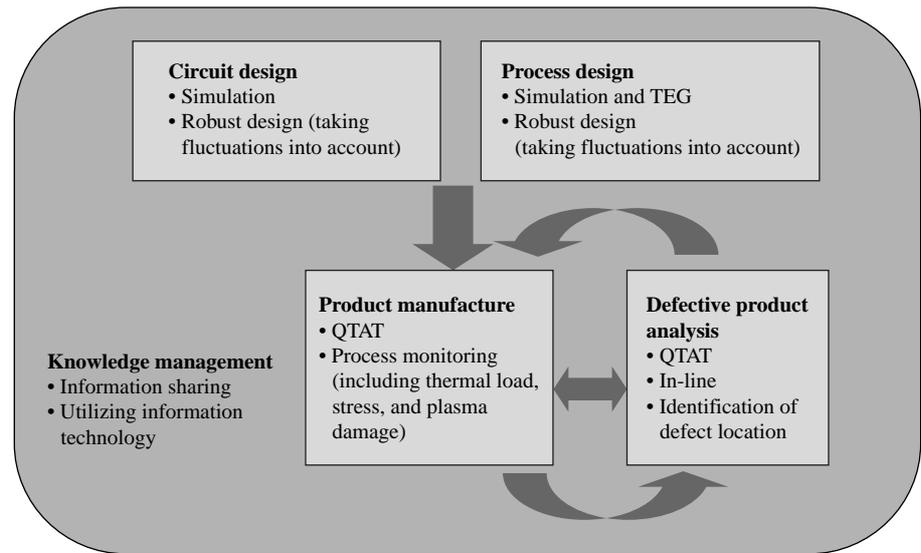
Fig. 7—Approaches to Shortening Development TAT.

As we progress toward the system on a chip, shorter development TAT to be able to cope with product diversification and changing production quantities and early improvement in yield in production is becoming increasingly important.

Circuit design
• Simulation
• Robust design (taking fluctuations into account)

Process design
• Simulation and TEG
• Robust design (taking fluctuations into account)

Knowledge management
• Information sharing
• Utilizing information technology

Product manufacture
• QTAT
• Process monitoring (including thermal load, stress, and plasma damage)

Defective product analysis
• QTAT
• In-line
• Identification of defect location

PRODUCTION TECHNOLOGY
Shorter Development TAT

As progress is made toward realizing the system on a chip, forms of production that can cope with diverse products and changing production quantities will become mainstream. A variety of LSI chips are developed in a short time and production period and production quantity depend on user requirements. Thus, shorter LSI development TAT and short-term improvement of yield in production are becoming increasingly important.

The important points concerning shorter development TAT are (1) concurrent development of circuits and processes that makes good use of TEGs (test element groups) and simulation, (2) robust circuit and process design that takes manufacturing fluctuations into account, and (3) defective product analysis and countermeasure prototyping by means of QTAT (quick TAT) (Fig. 7).

The repeated product prototyping for verification of circuit design and process design is problematic because of the time and expense it requires. It is therefore necessary to do sufficient design verification for these two types of design in parallel prior to product prototyping by using design CAD for circuit design prototyping and TCAD and TEGs for process design prototyping.

In circuit and process design, it is important to take manufacturing fluctuations into account in circuit simulation and device modeling and to estimate performance at time of manufacture with the aim of early improvement of circuits and devices.

Also, process monitoring by means of in-line measurement and analysis technology for the prototype process and early discovery of defects are essential. With the addition of plasma processing and the CMP process comes the need for monitoring the amount of charge-up and stress, which are device load parameters, as well as monitoring for high reproducibility.

For defect detection and location identification, it is important to make full use of rough position estimation by circuit design automation and direct measurement by means of analysis of light or heat emission, electrical potential contrast observation by means of SEM (scanning electron microscope) or FIB (focused ion beam), or nanoprobe (a device in which four scanning probes microscopes are installed within a SEM). Recently, the detection of defects that occur in complex structures that have a high integration scale and include new materials has become important. For example, the occurrence of microscopic voids in the plated film that is used for copper wiring is a concern with regard to reliability, and thus requires countermeasures. It is therefore essential to detect microscopic defects by using SEM inspection equipment, which can make comparative inspections between chips, even for random wiring patterns.

Cost Reduction

Important points in reducing cost are to consider cost beginning with the device process design stage and to increase the productivity of manufacturing technology. Together with decreasing the number of masks required in device processes, it is necessary to also increase the number of chips obtained per wafer.

The ways to increase the number of chips per wafer include (1) reducing the chip size, (2) expanding the area from which chips can be obtained on the wafer, and (3) increasing the wafer diameter.

Reduction of chip size is one of the reasons for using higher integration scales, and we believe it will continue to be promoted as a main factor in cost reduction. Furthermore, there is a need for effort to expand the wafer area on which chips can be formed by using various process treatments to extend the usable area in which uniformity is maintained to edge of the wafer.

The construction of a 300-mm-diameter wafer line for 0.1 μm-generation mass production is gaining stride. Production technology for 300-mm wafers will soon be established and the cost-reduction effect is expected to begin to appear. Efforts to cope with the change to 300-mm wafers have begun with the production facilities. In future, we also plan to extend it to an R&D line to ensure a smooth transition development and production technology.

It goes without saying that the facilities investment expense for manufacturing and inspection equipment bears heavily on manufacturing cost. In the field of manufacturing and inspection equipment, progress is being made in integration, which allows multiple processes to be performed with one system. Also important is serious reconsideration from the viewpoint of manufacturing cost as well as function so as to bring out cost advantages.

CONCLUSIONS

We have described semiconductor fabrication and inspection technology for 0.1 μm-generation devices.

As progress is made toward the system on a chip, it is becoming increasingly important to ascertain "What to make?" and proceed with technological development on that basis. Our approach is to provide the customer with the best solution by constructing new relationships of cooperation among the various technologies for design, device/process, and manufacture and inspection.

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