CPU Technologies for Networks and Multimedia

Kunio Uchiyama
Hirofumi Mukai
Ikuya Kawasaki
Tsuguji Tachiuchi

OVERVIEW: Hitachi has put the H8/300 and H8/300L series 8-bit microcomputers, the H8/300H, H8S/2000 and H8S/2600 series 16-bit microcomputers and the SuperH RISC engine series 32-bit microcomputer into commercial production to meet the various requirements placed on electronic appliances in the consumer product, information, communications and industrial fields. Upward compatibility is maintained throughout the H8/H8S series, from the H8/300L at the low end to the H8S/2600 model at the high end. The series includes inexpensive and reduced power consumption models with limited numbers of pins, the world's highest level CPU core for 16-bit microcomputer performance, large amounts of on-chip flash memory and a variety of peripheral modules, and allows you to select the combination that best suits your system. The SuperH RISC engine series allows you to freely select from among CPU cores with 26 to 360 MIPS (million instructions per second) performance based on our 16-bit, fixed-length instruction RISC (reduced instruction set computer) architecture. This series includes SH2-DSP/SH3-DSP models that incorporate DSPs (digital signal processors) and vector-type FPUs (floating-point units) for which there is strong demand from the network and multimedia fields. Hitachi has also developed the SH-5 with performance in the 1,000-MIPS class and an architecture expanded to 64 bits as the next-generation processor. Hitachi has also developed middleware for voice, image, audio and communications applications, to be run mainly on the SuperH RISC engines. It is very easy to construct products for network and multimedia applications on the basis of the middleware.

INTRODUCTION

MICROCOMPUTERS are used in a variety of electronic appliances in the consumer product, information, communications and industrial fields. These appliances have become more widely used as a result of the widespread use of the Internet and advance in multimedia, and the result has been a need for a more diverse range of microcomputers.

Hitachi has put the H8/300 and H8/300L series 8-bit microcomputers, the H8/300H, H8S/2000 and H8S/2600 series 16-bit microcomputers and the SuperH RISC engine series 32-bit microcomputers into commercial production to meet a variety of requirements for performance, price, power consumption and functionality (see Fig. 1).

We will also explain the current situation regarding our development of middleware, i.e., programs that are absolutely necessary for constructing systems around these CPUs (central processing units) and microcomputers, in view of the current trends in the twin areas of network and multimedia technologies.

H8/H8S SERIES

Product Development

Hitachi has commercially produced H8/300 and H8/300L series 8-bit microcomputers and H8/300H and H8S (H8S/2000, H8S/2600) series 16-bit microcomputers to meet various requirements for electronic appliances in the consumer-product, information and industrial fields (see Fig. 2). All of the series provide upward-compatibility at the object level, allowing easy migration to higher-level models when users require improved performance. The H8S series achieves the world's highest rate of operation

RISC: reduced instruction set computer
DSP: digital signal processor
MIPS: million instructions per second

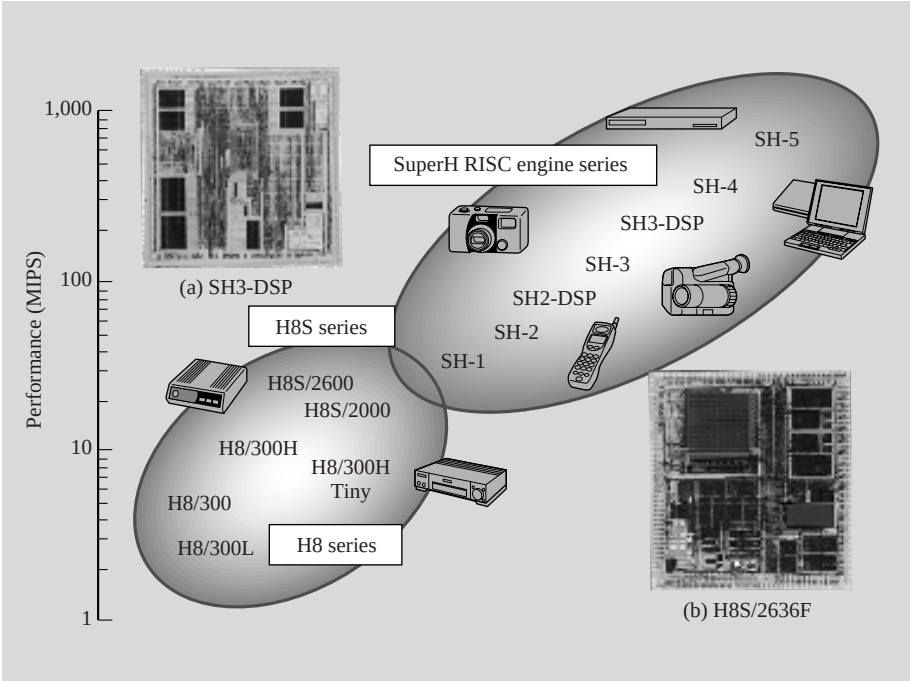

Fig. 1— Product Development of the H8, H8S and SuperH RISC Engine Series.
Hitachi has developed a wide range of CPUs, from the 8-bit H8 series to the 32- to 64-bit SuperH RISC engine series.

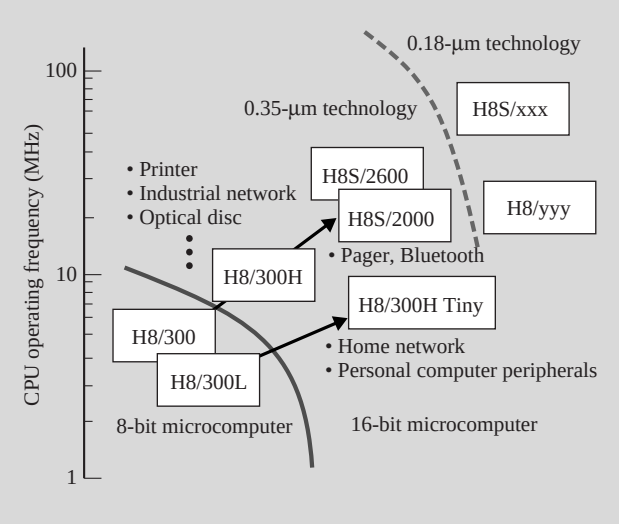

Fig. 2— Product Development and Major Applications of the H8/H8S Series.
The H8/H8S series meet the various requirements of electronic appliances in the consumer product, information, and industrial fields.

at 18.9 MIPS (for operation on 3.3 V at 33 MHz), where each basic instruction is executed within 1 cycle and the internal memory is accessed within 1 cycle. Products in the series are also able to execute multiplication and multiply & accumulate operations in 4 cycles. In both the H8 and H8S series, products are also available with internal flash memory (F-ZTAT, or Flexible Zero Turnaround Time versions). This allows programs to be written or modified on the board; the mass assembly lines can thus be simplified; and maintenance after shipment is easy. These products allow internal flash memory capacities of up to 512 kbytes.

Applications

Fig. 2 shows representative fields of application for each series. For the H8/300H Tiny series, Hitachi has succeeded in realizing a low price for a product with fewer than 64 pins. Products in the series can be configured to contain a variety of modules that represent intellectual property (IPs); the I^2C bus, the LPC (low pin count) bus advocated by Intel Corp., or the USB (universal serial bus) for application to home networks and personal computer peripherals. Products in the H8S/2000 series are ideal for use in mobile appliances that call for low power consumption. Typical applications include pagers, Bluetooth devices, MD (mini-disc) players, etc. The H8/300H and H8S/2600 series can be used in applications to do with optical discs [CD-R/RWs (compact disc, recordable/rewritable), DVD-ROMs (digital versatile disc, read-only memory)], printers, and automobile/industrial networks. An IP module for USB and CAN (controller area network) realizes a high-speed and highly reliable communications protocol, and is available for connection to the CPU cores of this series.

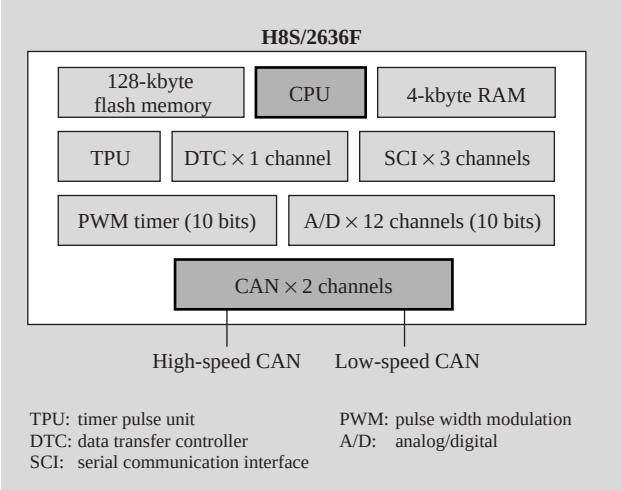

Fig. 3— Functions of the H8S/2636F for Controlling Automobile/Industrial Networks.
The H8S/2636F provides a gateway function for two CAN-interface channels.

Fig. 3 shows the functions of the H8S/2636F that is in commercial production as a product for the control of automobile/industrial networks. This microcomputer incorporates the high-speed CPU core of the H8S/2600 series and 128 kbytes of flash memory. It has two 1 Mbit/s CAN interface channels and is able to control high-speed and low-speed CAN buses as well as the interfaces required to exchange information on both buses.

SuperH RISC engine SERIES

Product Development

The SuperH RISC engine series, which is suitable for use in small mobile information appliances and digital appliances, was developed to meet requirements for well-balanced performance, power consumption and price. Fig. 4 shows the development of products in this series. Development of the CPU cores, from the SH-1 to SH-4 was based on a compact, low power consumption CPU with a 16-bit, fixed-length instruction RISC (reduced instruction set computer) architecture, to which a cache memory, an MMU (memory-management unit), a DSP (digital signal processor), an FPU (floating-point unit) and the superscalar method have been added. The architecture of the SH-5, designed for next-generation networks and multimedia products, has been expanded from 32 bits to 64 bits and uses SIMD (single instruction, multiple data) instructions. This series is also ideal for use in a variety of applications, thanks to product development that has covered a wide range of variants in terms of frequency, flash memory, ROM, RAM (random access memory), and peripheral functionality.

By 1999, Hitachi had shipped more than 100 million SuperH RISC engines. The series has been widely adopted for industrial, OA (office automation)/computer, consumer product, communications and automotive applications, and Hitachi intends to positively develop this series further in the future.

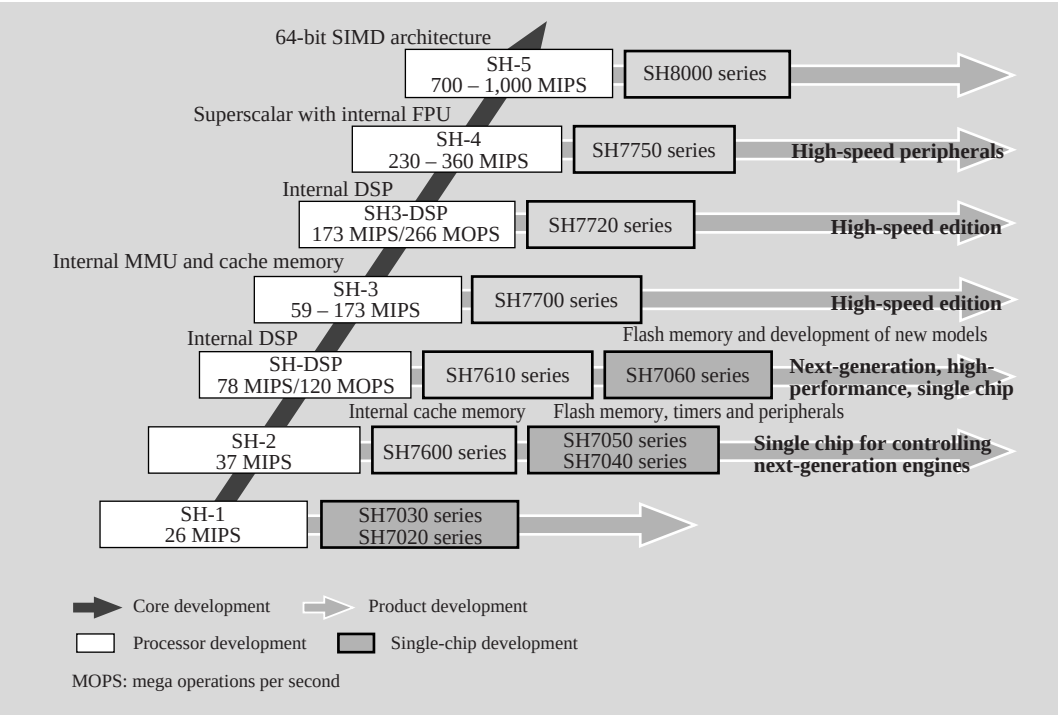

Fig. 4— Development of the SuperH RISC engine Series.
The SuperH RISC engine series provides a wide range of solutions for network-related and multimedia equipment.

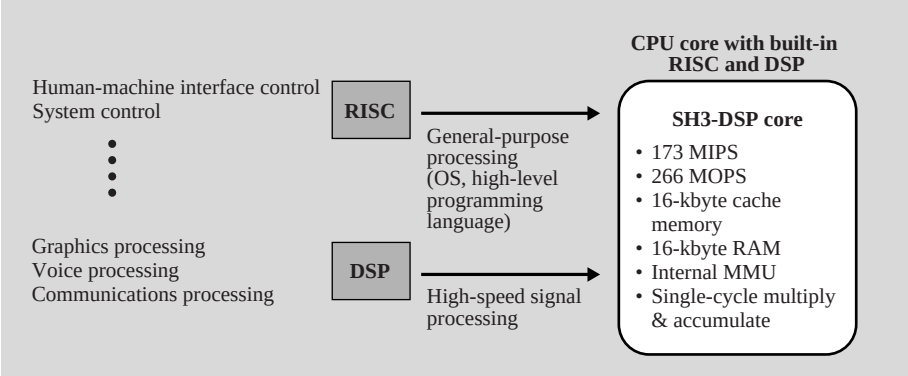

Fig. 5— Design Concept of the SH3-DSP.
The SH3-DSP architecture incorporates both RISC and DSP units, allowing the efficient execution of both general-purpose and signal-processing operations by the CPU.

MH: modified huffman
MR: modified read
MMR: modified modified read
PIAFS: personal handyphone system Internet access forum standard
ADPCM: adaptive differential pulse code modulation
JBIG: joint bi-level image experts group

* Java, and all trademarks and logos related to Java, are trademarks or registered trademarks of Sun Microsystems, Inc. in the U.S.A. and other countries.

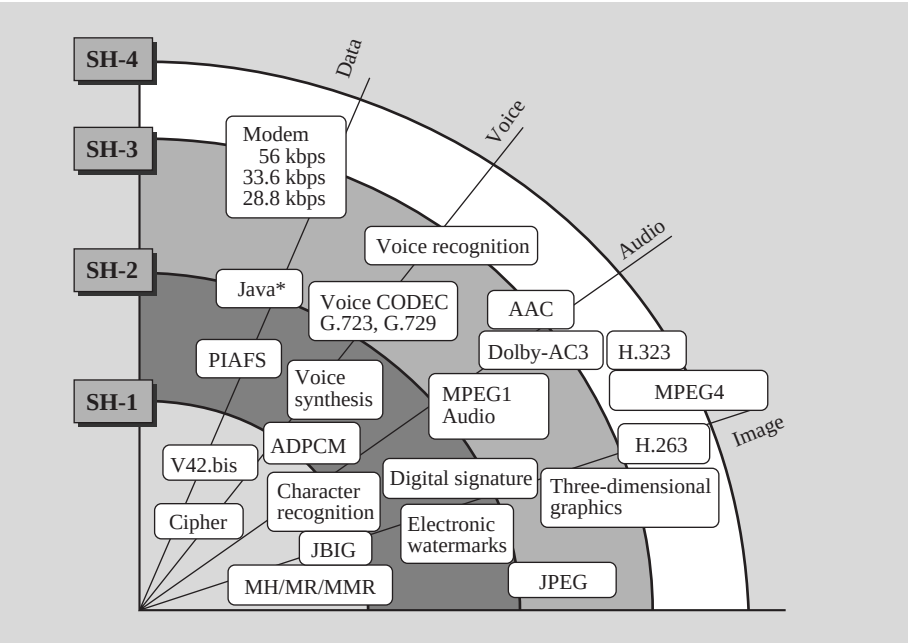

Fig. 6— Development of Middleware Products.
A variety of middleware has been provided for use with the SuperH RISC engine series and eases the development of appliances.

An Architecture for Multimedia and Its Applications

Hitachi has developed the SH3-DSP that is suitable for application in networks and multimedia. In today's Internet society, multimedia products require RISC microcomputers to control both the human-machine interface and the system, and DSPs to process image and voice signals. The SH3-DSP was developed by integrating the RISC and DSP in the CPU core, realizing strong performance and low power consumption (see Fig. 5). This CPU has a built-in cache memory and MMU and supports Windows CE* and many other operating systems. It also has a processing function that is equivalent to a general-purpose DSP and executes middleware for operation as a software modem, voice synthesizer, voice/image CODEC, etc., at high speed. In various multimedia applications, it achieves a performance better than two or three times that of an SH-3 running at the same frequency. Applications include pocket personal computers, modems and digital still cameras.

*Windows is a registered trademark of Microsoft Corp. in the U.S.A. and other countries.

MIDDLEWARE

Hitachi has developed the following middleware for applications in the network and multimedia fields. These modules are mainly intended for the SuperH RISC engine series (see Fig. 6), and enable the easy construction of customer systems.

(1) Image middleware such as JPEG (joint photographic expert group) for encoding and decoding still images used for digital cameras and MPEG4 (moving picture expert group 4) for encoding and decoding motion pictures.

TABLE 1. Programming Results for the Voice CODEC
The architecture of the SH2-DSP/SH3-DSP with its RISC and DSP realizes an efficient voice CODEC.

Method	G.711	G.726	G.729A
Program size	1 kbyte	2 kbytes	26 kbytes
Required data memory	256 bytes	1 kbyte	7 kbytes
Required frequency (MHz)			
Encoding	0.1	12	22
Decoding	0.1	12	5

(2) Audio middleware such as AAC (advance audio coding), Dolby-AC3 (audio code number 3) and MP3 (MPEG1 audio layer 3) used for solid audio.
(3) Voice-related middleware for voice recognition and synthesis for car navigation systems, and for voice encoding and decoding for use in Internet telephony.
(4) Data communications middleware such as 56-kbps modem module.

A practical example of using a voice CODEC with the SuperH RISC engine is described below. With the advent of the Internet, data is easily transmitted worldwide and there are great expectations for the transmission of voice signals via a voice CODEC called the VoIP (voice-over-Internet protocol). Table 1 shows the results of programming according to three voice CODEC methods (G.711, G.726 and G.729A) developed for the SH2-DSP and SH3-DSP. Both architectures, with their combination of RISC and DSP, enable G.729A transmission of high-quality voice signals at a high compression ratio with processing of the data at a rate below 30 MHz per channel.

CONCLUSIONS

We have outlined Hitachi's CPU technologies for network and multimedia applications. In this field, appliances must meet a variety of requirements. These include high levels of performance in handling multimedia data and in network control, and low power consumption. Appliances must fulfill these requirements at a low price. Hitachi intends to further develop all of its microcomputer product ranges, from the H8/H8S series to the SuperH RISC engine series, and provides flexible ways of satisfying the above needs and meeting the requirements of customers.

ABOUT THE AUTHORS

Kunio Uchiyama
Joined Hitachi, Ltd. in 1978, and now works at the System LSI Research Department, Central Research Laboratory. He is currently engaged in the research and development of microprocessors. Mr. Uchiyama can be reached by e-mail at uchiyama@crl.hitachi.co.jp.

Hirofumi Mukai
Joined Hitachi, Ltd. in 1984, and now works at the Business Unit 9, Semiconductor & Integrated Circuits. He is currently engaged in the development of the H8/H8S series. Mr. Mukai can be reached by e-mail at mukai-hirofumi@sic.hitachi.co.jp.

Ikuya Kawasaki
Joined Hitachi, Ltd. in 1982, and now works at the Mobile LSI Processor 1st Design Department, Mobile LSI Business Unit, Semiconductor & Integrated Circuits. He is currently engaged in the development of the SuperH RISC engine series. Mr. Kawasaki can be reached by e-mail at kawasaki-ikuya@sic.hitachi.co.jp.

Tsuguji Tachiuchi
Joined Hitachi, Ltd. in 1974, and now works at the Middleware Development, Software Technology Division, Software & Hardware Technologies, Semiconductor & Integrated Circuits. He is currently engaged in the development of voice CODEC and image-handling middleware. Mr. Tachiuchi can be reached by e-mail at tachiuchi-tsuguji@sic.hitachi.co.jp.