Process Technologies for System LSI Chips

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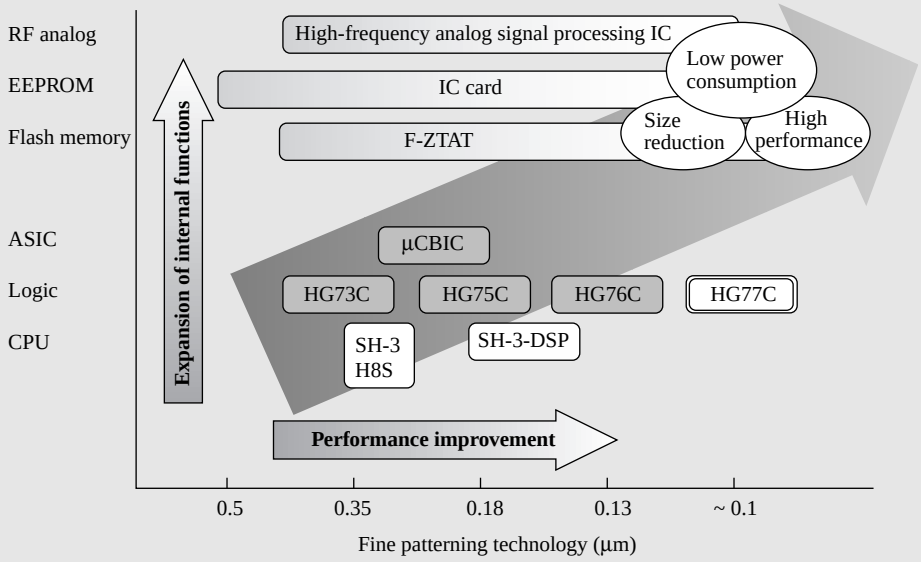
OVERVIEW: To produce systems-on-a-chip for the ever expanding range of multimedia and mobile communication applications, it is absolutely necessary to develop technologies for finer patterning and other new process-related technologies, so as to make the systems more efficient, less power consuming, and smaller. Hitachi developed these technologies prior to the 0.13-μm technology node and succeeded in producing prototype high-performance transistors. Hitachi will embody this technology in a platform then use it to develop high-frequency LSI chips, analog signal processing LSI chips, memory-embedded LSI chips, and many other products, in response to the enormous demand for digital information equipment.

INTRODUCTION

AS the demand for mobile terminals for Internet access and telecommunications has spread, the demands for more powerful, less power consuming, and smaller LSI chips have increased. Since finer patterning of semiconductor devices fulfills all of these demands, the history of semiconductor devices has mirrored that of fine patterning technology (see Fig. 1). In the process, the gate length, which determines the performance of transistors, has been reduced to one tenth of its value 15 years ago. Although road maps for progress in fine patterning used to be set by individual companies, standard road maps have come to be used. This is because they allow a more efficient approach to the development of semiconductor technology and semiconductor production equipment. One such road map is the ITRS (International Technology Roadmap for Semiconductors). Table 1 shows the items listed in the ITRS that are relevant to systems-on-a-chip.

According to the ITRS, 0.13-μm LSI chips will enter commercial production in 2002, the shortest gate



RF: radio frequency
DRAM: dynamic random access memory
CPU: central processing unit
F-ZTAT: flexible zero turnaround time
EEPROM: electrically erasable programmable read-only memory
ASIC: application specific IC
DSP: digital signal processor
μ CBIC: micro cell based IC

Fig. 1— Development of System LSI Chips by Hitachi. Hitachi has employed process technologies for embedding memories and analog devices as well as the most advanced CMOS (complementary MOS) transistors, in order to increase the performance and reduce the power consumption and sizes of systems-on-a-chip, centered on SuperH series RISC (reduced instruction set computer) devices.

TABLE 1. ITRS in Relation to Systems-on-a-Chip (1999 edition)
The ITRS predicts that the 0.13-μm technology node will start in 2001-2002.

Item \ Year	2000	2001	2002	2003	2004
Gate length (MPU) (nm)	120	100	85	80	70
Supply voltage (V)	1,5 to 1.8	1,2 to 1.5	As on the left	As on the left	0.9 to 1.2
Drive current (μA/μm)	750/350	As on the left	As on the left	As on the left	As on the left
OFF-state current (μA/μm)	7	8	10	13	16
Gate-insulating film thickness (nm)	1.9 to 2.5	1.5 to 1.9	As on the left	As on the left	1.2 to 1.5
Intermediate wiring pitch	450	405	365	330	295

MPU: microprocessing unit

lengths of transistors will reach 85 nm, and the shortest wiring pitches will be 0.36 μm.

In this article, we will explain the main process technologies required in the coming age, the characteristics of a prototype transistor produced using these technologies, and the high-frequency LSI chips (ICs) and LSI chips with built-in memory that are, along with the CMOS (complementary metal-oxide semiconductor) transistors[1)] themselves, essential for mobile terminals.

HIGH-PERFORMANCE CMOS TECHNOLOGY (0.1-μm TRANSISTOR)

Fine patterning technologies such as lithography and precision dry etching are essential in forming gate electrodes with dimensions as short as 85 nm. It is also necessary to reduce the thickness of the gate-insulating film and the depth of the source-drain junction in the vertical direction. The thickness of the gate insulating film must be reduced so that it is possible to obtain the driving current by increasing the gate capacitance, and to prevent the short-channel effect. The shallow junction is also required to prevent the short-channel effect.

The leakage of direct tunneling current from the gate penetrates the gate-insulating film. Since the gate-insulating film will become as thin as 2 nm, this will become impossible to ignore. To avoid this problem, the film of silicon oxide that is currently used must be replaced by a film of a material that has a higher dielectric constant. It will also be necessary to realize a larger capacity with a thicker film. To form diffusion layers thinner than 50 nm while maintaining a low resistance, a new technology will have to be introduced.

The following explains the main process technologies required to realize transistors with a gate length of 85 nm.

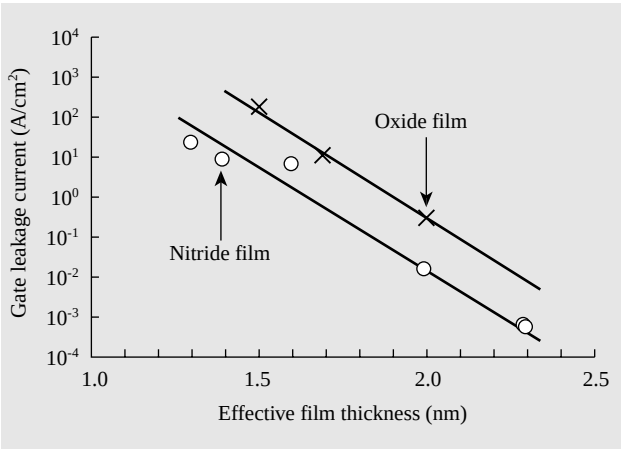


Fig. 2— Gate-Leakage Currents Through Oxide and Nitride Films.
We confirmed that nitride film reduced leakage currents to about 10% of that of conventional oxide film.

Silicon-Nitride Gate Insulating Films

The dielectric constant of a film of silicon nitride is about twice that of a film of silicon oxide. A given film of silicon nitride will thus produce a gate capacitance equivalent to that produced by a film of silicon oxide that is only half as thick. A thicker film is able to prevent current leakage from the gate. Fig. 2 shows effective film thickness dependability for both oxide and nitride films. Nitride film reduces leakage current to 10% of the value for an equally thick oxide film.

Gate-insulating nitride film is effective in restricting "boron leakage" that is caused by the pMOS (p-channel MOS) elements of the CMOS transistors. In boron leakage, boron penetrates the oxide film and enters the channel area when gate electrodes that contain a lot of boron are heat-treated. This causes the problem of increased dispersion of threshold-voltage values. Nitride film prevents leakage, since it is hardly penetrated by boron. According to the results of our

experiments, the thickness of nitride film used can thus be reduced by about 0.2 nm more than oxide film of a dielectrically-equivalent thickness. The effective film thickness was 1.9 nm in our trial production.

Technology for Forming Shallow Junctions

As mentioned above, the source-drain junction must be formed shallow, to prevent the short-channel effect. However, the source resistance must not be increased so much by the shallow junction that it becomes impossible to obtain a high driving current. A technology for forming high-density shallow junctions is thus required. Low-energy ion implantation is a suitable way of achieving this, as the implanted impurities remain near the surface. High-temperature heat treatment is also necessary to reduce the resistance of heavily doped layers. However, since the impurities then move and a deeper junction is formed as a result of this heat treatment, the heat treatment must be applied over a short period, to keep the junction shallow.

In producing our trial device, we used a low level of energy, below 5 keV, to implant the ions, and applied heat treatment at 1,000 °C for 10 seconds. As a result, we were able to realize a shallow source-drain structure with a junction depth of about 50 nm.

Photo-Lithography

The most important factor in making finer patterning practical is photo-lithographic technique. The optical wavelength must be shortened and the lens aperture increased to resolve finer patterns. A KrF excimer laser with a wavelength of 248 nm was adopted for the present generation of 0.18-μm products. It is predicted that an ArF excimer laser with a wavelength of 193 nm will be used for the next generation.

Such super-high-resolution technologies as phase-shift technology, technology for correcting the optical proximity effect and zonal lighting technology can form patterns finer than the limit of the exposure tool. At Hitachi we have formed patterns equivalent to the resolution obtainable with an ArF excimer laser by using a KrF excimer laser and super-high-resolution technologies. The wiring pitch was 0.36 μm and the gate length was 0.1 μm (the equivalent figures for a standard method of exposure are 0.4 μm and 0.15 μm, respectively) (see Fig. 3). It is possible to apply these technologies to ArF lithography, and sizes below the limit of the exposure tool will again be obtained.

We have explained the main technologies used to reduce transistor sizes. We explain some of our other process technologies in the other articles in this issue.

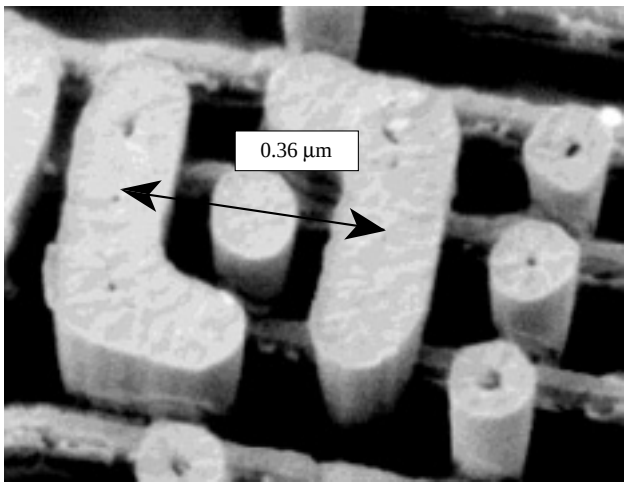


Fig. 3— Bird's-Eye View of an SRAM (Static Random-Access Memory) Cell.
Hitachi achieved a wiring pitch of 0.36 μm by using a KrF excimer laser based on phase-shift technology.

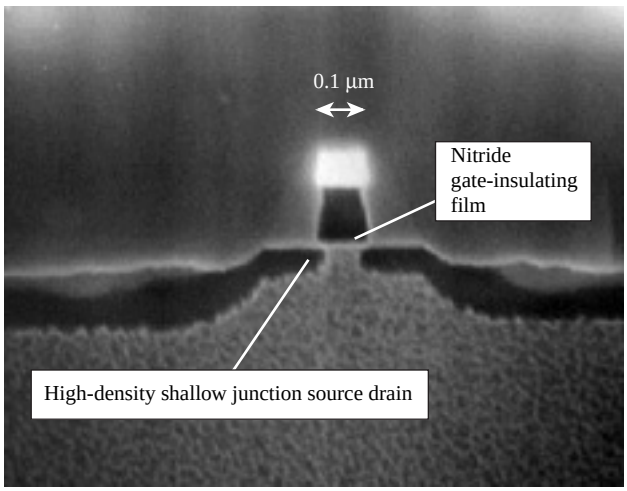


Fig. 4— Section Through a 0.1-μm Transistor.
Hitachi achieved a 0.1-μm gate length by using a nitride gate-insulating film and by forming a high-density shallow junction.

Transistor Characteristics

Fig. 4 is a cross-sectional view of one of our prototype transistors. The design attained large currents of 1,000 μA/μm for an nMOS (n-channel MOS) device and 430 μA/μm for a pMOS device. The threshold voltage did not drop until the gate length reached 0.1 μm or shorter, and the vertical scaling restrained the short-channel effect (see Table 2).

In the future, we will integrate a version of this transistor with even better performance, for incorporation in commercial products.

TABLE 2. Transistor Characteristics
Hitachi has been able to achieve a better performance than that of a 0.1-μm transistor on the ITRS roadmap (see Table 1).

Gate length (μm)	0.1		
Thickness of gate-oxide film (nm)	2.8		
Supply voltage (V)	1.5		1.2
Drive current (n) (μA/μm)	900	950	620
Drive current (p) (μA/μm)	370	404	230
OFF-state current (nA/μm)	1	3	1

LSI CHIPS FOR DIGITAL INFORMATION EQUIPMENT

Hitachi has used the following technologies to develop high-performance, low-power consumption and low-cost systems-on-a-chip for use in mobile terminals and other digital consumer-electronic items of in the digital information age.

Nonvolatile Device Technology

An embedded small-capacity flash memory is the main way of storing programs in the microprocessors of portable information equipment. Hitachi used the 0.35-μm process and developed an F-ZTAT (flexible zero turnaround time) microcomputer with 48 kbytes of embedded flash memory, the core of which was an SH-DSP 32-bit RISC (reduced instruction set computer) processor. The F-ZTAT microcomputer allows the writing of on-board programs, the development of programs, and the production of samples, all at the same time, and this helps to reduce development times. We were able to increase the speed of reading by dividing the bit line and improving the sense amplifier. At the same time, we developed transistors with gate-oxide films of two thicknesses, so as to better utilize the performance of these circuits. The development of a 0.2-μm F-ZTAT technology has improved performance even further.

Larger-capacity flash memories have, on the other hand, been used as media-storage devices for portable information equipment. Hitachi has developed an AND-type flash memory for high-speed writing and the multi-valued cell method for large capacities.[2)] This method is applied by the precise control of thresholds and the use of dispersion-reducing technology. The key technology is the forming of high-quality tunneling films that cause little electronic trap.

In the IC-card field, technology for producing nonvolatile memories that are highly secure, highly reliable, and high degree of integration is essential. Hitachi has met customers' requirements with an EEPROM (electrically erasable programmable read-only memory) based on its proprietary MONOS (metal-oxide nitride-oxide semiconductor) structure. For contactless cards, Hitachi is attempting to bring PZT (a compound of lead, zirconium, and titanium oxide) ferroelectric memory technology into practical use. Embedded DRAM process technology has also been developed to satisfy the requirement in the field of graphic processing for mobile terminals.

Analog Signal Processing IC

ICs for mobile communications and cellular phones must have good high-frequency characteristics and low-noise properties as well as having few parts, being compact, and consuming little power. To reduce numbers of parts, Hitachi has modified most parts in the RF (radio frequency) section to fit onto a single chip. Hitachi has also embedded bipolar devices on an SOI (silicon-on-insulator) board to develop 0.35-μm BiCMOS (bipolar-CMOS) devices, the parasitic capacitance of which was reduced to one tenth of conventional capacitance. The result is the HD155131TF a commercially produced high-speed, low-noise analog signal processing IC. We have also developed a self-aligning technology, in which IDP (in-situ phosphorus doped polysilicon) is used to form the base emitter portion and improve the high-frequency characteristics of the bipolar transistor[3)] (see Fig. 5). In order to further improve device characteristics, a SiGe transistor has also been developed.

High-Frequency Power Amplifier (RF Power Module)

Hitachi has developed an RF power MOSFET (MOS-type field-effect transistor) as a power amplifier for cellular phones. CMOS technology is applied in this transistor so that it operates very efficiently at low voltages. We used an offset-gate structure in order to reduce the ON resistance and, at the same time, achieve a high breakdown voltage. We also developed an Al short-circuit silicide gate structure for this transistor,

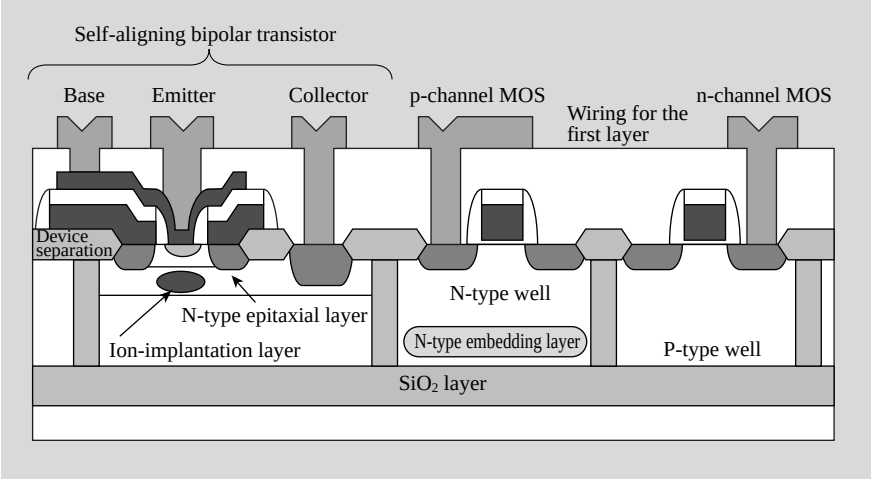


Fig. 5— Cross-Sectional View of an Analog Signal Processing One-Chip IC. Most parts of the RF section of the chips were modified in order to reduce the number of parts and cut costs. Good high-frequency characteristics were also obtained by applying IDP technology to the bipolar section.

in order to reduce gate resistance. The transistor performed well at high frequencies of up to 2 GHz. In order to further improve the transistor's high-frequency characteristics, we have developed a technology for thickening the gate-oxide film at the gate edge in a self-aligned manner. When GaAs devices are used with the W-CDMA (wideband code-division multiple access) system, more highly efficient and inexpensive high-frequency devices will be developed.

CONCLUSIONS

We have explained the process technologies used to develop state-of-the-art CMOS transistors and systems-on-a-chip that support the quick expansion of the market for digital information products.

Hitachi intends to further promote technical development in this area and continue to provide semiconductors that meet the requirements of customers.

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