Semiconductor Assembly Technologies for the Network Era

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OVERVIEW: The network era of the 21st century requires that both desktop-type equipment and mobile equipment be connected to networks for the exchange of data and information. Improvements to hardware, in the form of higher speeds of data transmission and information processing, will be required. Furthermore, higher-density assembly and lower levels of power consumption will be called for to realize lighter and more compact mobile equipment. Consequently, the semiconductor assembly technology for such equipment will not be the conventional surface mounting technology. Hitachi has been focusing on the development of a new assembly technology to meet these needs.

INTRODUCTION

IN the 21st century, remarkable changes are going to occur with respect to the semiconductor assembly technology used to produce equipment for network applications. Mobile equipment will be required to be lighter and more compact, whereas servers and routers will require faster processing and higher densities of assembly.

The following explains Hitachi's semiconductor assembly technology that will be used to meet these needs, centering on the cellular phone, which is expected to lead the way in high-density assembly technology.

TRENDS IN ELECTRONIC EQUIPMENT AND THE NEED FOR NEW ASSEMBLY TECHNOLOGY

Network equipment will be required to process data that represents sound, still pictures, and moving pictures, in addition to conventional character-based information, driving the development of semiconductor devices that handle more bits at higher rates. Some assembled equipment will also be required to be more compact, lighter, have a higher density, and be more reliable, and this will make adjustments to methods of assembly necessary (see Fig. 1).

In particular, the cellular phone is setting the pace

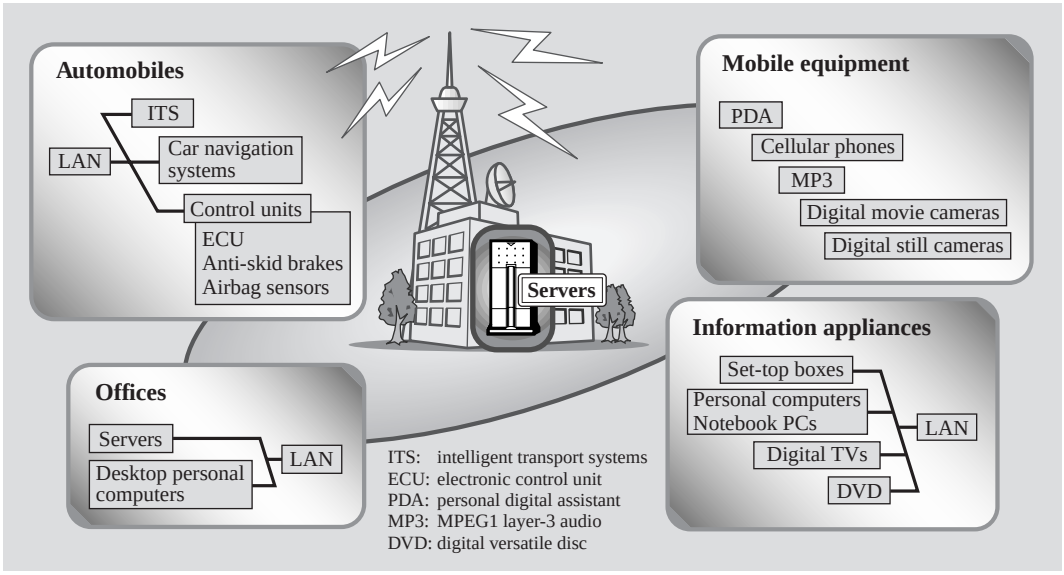


Fig. 1— The Variety of Digital Equipment Used in the Emerging Network Society. Terminal equipment can be divided into four main fields. The base station is the information source and creates a whole.

for assembly technology. Cellular phones are composed of a high-frequency section, a baseband section and a power-supply section. They have already been made more compact and lighter, and the assembly technology has been modularized for the high-frequency section while CSP (chip-size package) technology has been applied for the baseband section. MCM (multi-chip module) technology is also being used. In the future, since the cellular phone will function as a terminal for mail, music, and moving pictures, denser assembly, more systematization, and faster operation will all be required.

HIGH-DENSITY ASSEMBLY TECHNOLOGY FOR SYSTEMATIZATION

HPA Assembly Technology for Cellular Phone

Fig. 2 shows the trend in the miniaturization of Hitachi's HPA (high power amplifier) packages. In order to decrease heat resistance, the H1-PKG has a double-sided thick-aluminum-film printed-circuit board and a copper heat sink.

A glass ceramic multi-layered board was adopted for the latest K-PKG. Its structure includes thermal vias to reduce thermal resistance. The package's exterior has a leadless structure for surface mounting, and the passive components such as resistors, capacitors, etc. were reduced from the conventional 1608 size ($1.6 \times 0.8 \times 0.8$ mm) to 1005 size ($1.0 \times 0.5 \times 0.5$ mm) for a higher density of assembly. Changing the package's structure and adopting the higher-density assembly technology reduced the volume of the package to one quarter of its earlier value, from 0.8 m*l* for the H1-PKG to 0.2 m*l* for the K-PKG. In the future, we intend to develop a yet smaller type, the P-PKG, and to modularize the circuits around the HPA to create an MCM.

Packages of Discrete Semiconductors for Power Supplies

Battery-powered portable information terminals like cellular phones are required to run for hours after being charged, and incorporate circuits to reduce the burden on the battery. A power MOS-FET embedded on a SOP (small outline package) is used to control the power supply. Since high-speed processing and reduced power consumption have been in demand lately, Hitachi has developed a new LFPAK (loss-free package) to realize a low on-resistance and a high speed of operation (see Fig. 3). The LFPAK was structured with the conducting electrode plate connected directly to the silicon (a wire-free structure), the resistance and inductance contributed by the wiring were thus reduced to a minimum, and the on-resistance and package thickness were reduced to about 20% and 1.1 mm, respectively. Thermal resistance was also greatly improved by locating the drain terminal on the rear external surface and by adopting a lead-free surface treatment for the electrodes.

In the future, we intend to further develop the LFPAK lineup for various power requirements and to further promote CSPs, with the aim of achieving even better performance.

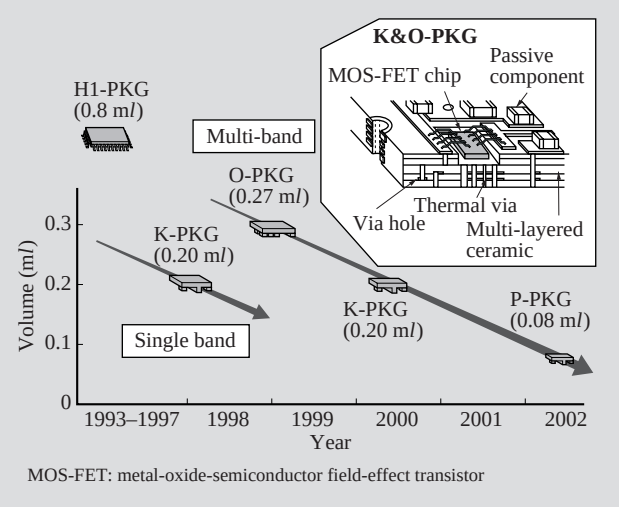


Fig. 2— Trends in High-Frequency Semiconductor Packaging. Modularization of the high power amplifiers of cellular phones has contributed to a reduction in the overall number of parts and eased design for assembly.

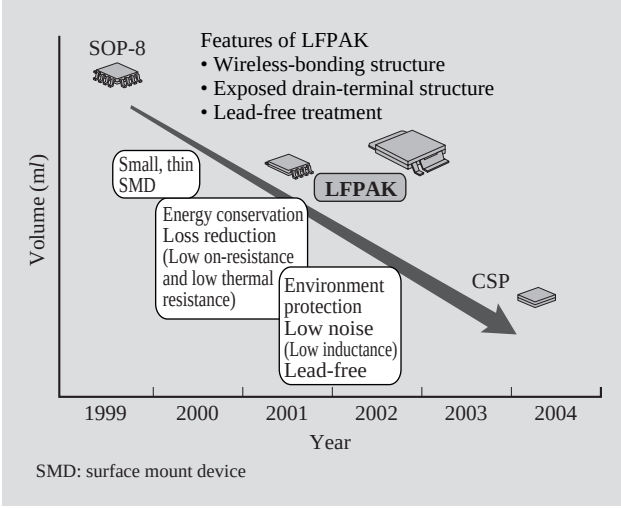


Fig. 3— Development of Power Transistor Packages. Hitachi has designed a small, high-performance power-transistor package to extend the battery lives of portable equipment.

Microcomputer and ASIC Assembly Technology

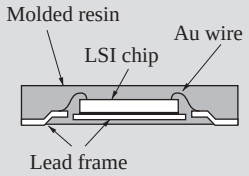
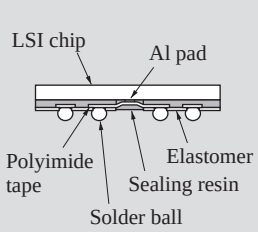
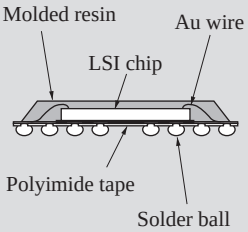
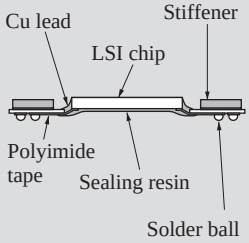
We have developed CSPs for portable items such as cellular phones, digital cameras, and digital movie equipment. Various types, suitable for devices ranging from small pin-count analog devices and memories to large pin-count microcomputers and ASICs (application-specific ICs) are available. Table 1 shows the structure and features of the CSP.

The CSP is designed to (1) make the external dimensions of the packaged device smaller, (2) be suited to conventional assembly technology, and (3) secure strength after assembly on the mother-board.

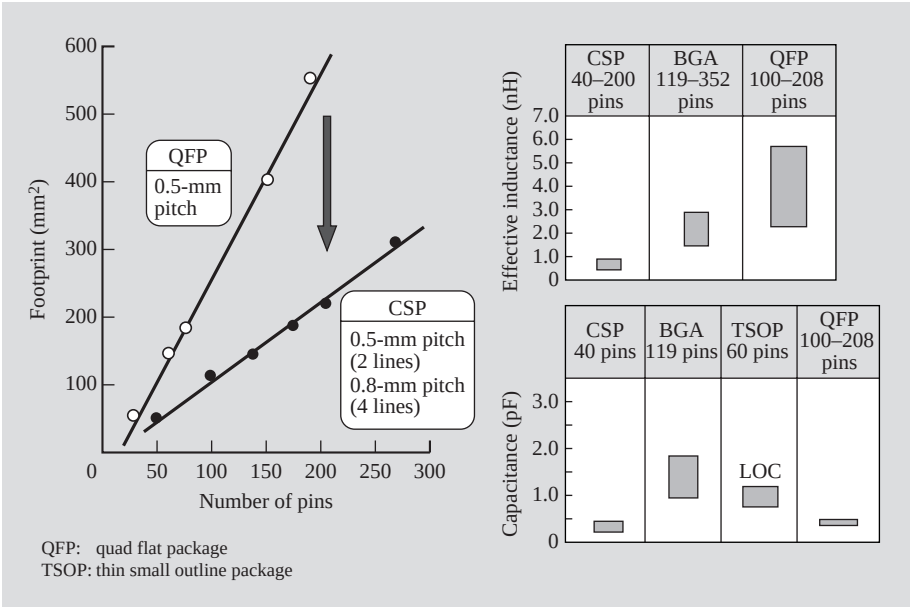
The new CSP allows the assembly area to be reduced to half that for a conventional package (see Fig. 4). Its low inductance and capacitance make high-speed operation possible. In the future, we intend to develop a finer-pitched CSP to further miniaturize devices in such packages.

TABLE 1. Structures and Features of CSPs[1, 2)]

In addition to the small lead-frame type CSP, there are three kinds of tape and substrate type CSP, handling the range from relatively few to very many pins.

Package name	QFN type	Fan-in type	Fan-in/out type	Fan-out type
EIAJ name	P-VQFN	T-TFBGA	T-TFBGA	T-TFBGA
Number of pins	< 60	< 100	80 to 200	200 <
Packaged devices	Analog device	Memory	Memory, microcomputers, ASICs	Microcomputers, ASICs
Structure				
Features	• Low cost	• Same area as the chip • Highly reliable connections	• Small • Low thermal resistance	• Applicable to multiple pins • Highly reliable connections

EIAJ: Electronic Industries Association of Japan
QFN: quad flat nonleaded



QFP: quad flat package
TSOP: thin small outline package

Fig. 4— Numbers of Pins, Footprints, and Electrical Performance of CSPs and Other Packages.
The CSP has a small footprint and electrical characteristics that are vastly superior to those of other packages. The CSP is thus suitable for use in portable equipment and with high-speed semiconductor devices.

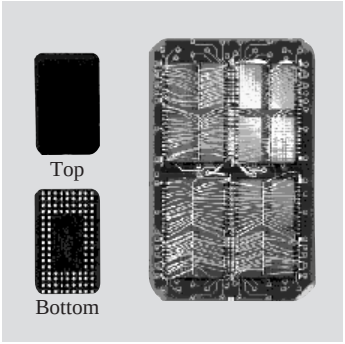


Fig. 5— Applying an MCP to Realize Multi-Bit Memory. Hitachi has developed a form of high-speed, multi-bit memory in which several chips are placed on a multilayered substrate.

High-Density Packaging Technology to realize Multi-Bit DRAMs

Since the need to process images has increased lately, the demand for wide-bus DRAMs (dynamic random access memories), for use in digital cameras and other equipment, has increased. Hitachi has developed 32-bit and 64-bit buses by embedding more than one DRAM on BGA (ball-grid array) and CSP boards. Fig. 5 shows the package for a 64-bit wide bus.

3D Packaging Technology

Hitachi has developed a method of assembling chips in multiple layers in packages by employing technology for higher densities of assembly. We developed the following as sub-systems for high-density assembly: (1) packages with multiple layers of logic and memory in a single QFP, (2) packages with multiple layers of DRAM or flash memory in a single TSOP, (3) packages with thin chips, including flash memory and SRAM (static RAMs) in a single CSP.

System Packages (Flip-Chip/MCM Technology)

We have been reviewing the MCM with respect to higher densities of assembly, application to high-speed circuits, and the reduction of development periods. Since the COB (chip-on-board)-MCM, which Hitachi currently produces commercially, requires a connection area as well as the area of the chip itself, it is the largest of the MCMs. Since wire bonding is used in this MCM, it is also unsuitable for use with high-speed bus circuits. In order to further reduce the module's size and make it suitable for high-speed processing, we have developed the "ACF-MCM," in which Au bumps are formed on the chip's bonding pads and ACF (anisotropic conductive film) is used to assemble them on the MCM. Fig. 6 shows a product with a 32-bit bus that contains one SH-4 microcomputer and four DRAM ICs, and which operates at 100 MHz. Since the chip's pad pitch is 80 μm, a built-up substrate is used.

The need for greater numbers of pins has increased with the need to handle wider ranges and higher levels of functionality. We have thus also developed the WPP (wafer process package)-MCM, using WPP technology to take connection terminals from all faces of the chip (see Fig. 7).

ADAPTING TECHNOLOGY TO THE ENVIRONMENT

We have also reviewed the solder materials we had been using in assembly, in order to reduce the burden on the environment. The following obstacles to establishing a lead-free assembly technology were encountered: (1) developing a substitute for lead and

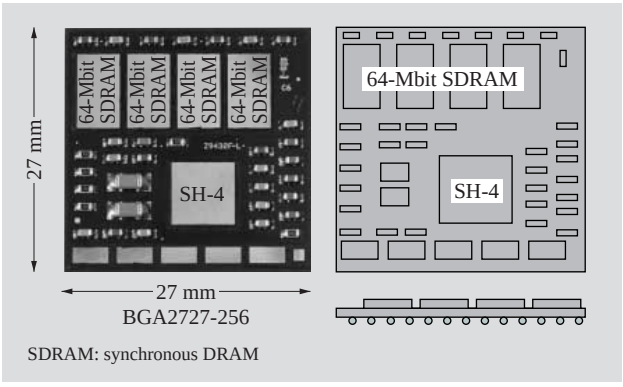


Fig. 6— Typical MCM with Embedded SH-4 Microcomputer. We were able to realize a compact, highly reliable MCM by effectively combining an ACF and substrate material.

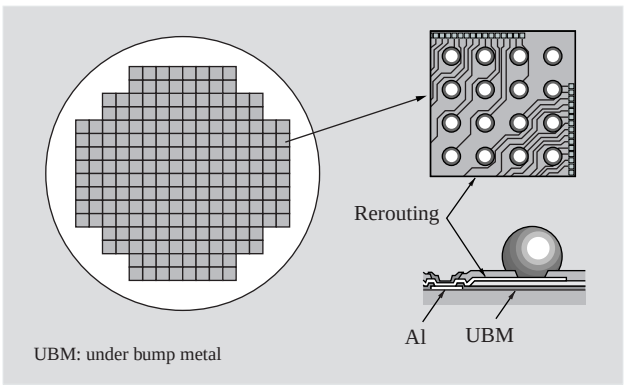


Fig. 7— Overview of WPP Technology. We produced area array bumps by combining Cu wiring and solder bump technology. This resulted in the development of small, multiple-pin flip chips.

(2) improving the heat resistance of packages.

Hitachi has been selecting new solder materials in cooperation with the industry as a whole. We adopted the Sn-Bi system or Pd as the solder material for use in the surface treatment of package leads, and the Sn-Ag system for BGA and CSP balls. On the other hand, since Sn-Ag system materials are mainly used for board assembly and have melting points 20–30˚C higher than their eutectic temperatures, the resistance of the packages to heat must be improved. The LOC (lead-on-chip) structure or the SDP (small die pad) structure has been adopted for most of the conventional surface-assembled packages, such as TSOPs and QFPs. Both structures have been confirmed as highly heat-resistant. We now expect to improve the heat resistance of CSPs after reviewing the materials used.

CONCLUSIONS

Semiconductor assembly technology for the network era has been reviewed. Since there is an increasing need for a more diverse range of board assembly technologies for electronic equipment and high-speed circuits, packaging technology will change greatly. In the future, we intend to improve our CSP lineup for a variety of mobile equipment, including cellular phones, and develop packaging technologies for the currently most promising flip-chip forms of assembly, and also develop simulation and design technologies for high-speed circuits, including for the mother-board.

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