Inspection-analysis Solutions for High-quality and High-efficiency Semiconductor Device Manufacturing

Kenji Watanabe, Dr. Eng.
Aritoshi Sugimoto
Mari Nozoe

OVERVIEW: Volume production of 90-nm node semiconductor products began in 2003, and research has been already well advanced on products for the next-generation 65-nm technology node. As feature sizes descend further into the deep submicrometer range, it becomes increasingly important for maintaining quality and streamlined production to exploit a range of analytical tools that are tightly integrated as a total system including (1) CD-SEM (critical-dimension scanning electron microscope) and other metrology tools, (2) defect inspection tools, (3) data collection and analysis systems, (4) SEM and TEM (transmission-electron microscope (TEM) analytical tools, and more. Hitachi Group is known for its lineup of leading-edge, high-performance metrology, inspection, and analytical tools for present and future technology nodes, but goes even further in providing inspection and analysis solutions that are tailored to the very diverse needs of individual device manufacturers.

INTRODUCTION

OVER the past several years, successive generations of semiconductor device geometries have been shrinking at a rate of one generation every two years, with 0.13-μm node devices going into production in 2001. Although this phenomenal pace is beginning to abate somewhat[1)], production of 90-nm-node devices began in 2003, and development of 65-nm-node parts is already well advanced[2, 3)]. Basic challenges in the mass production of semiconductor devices are to set up production processes while working through a succession of preproduction samples within a very

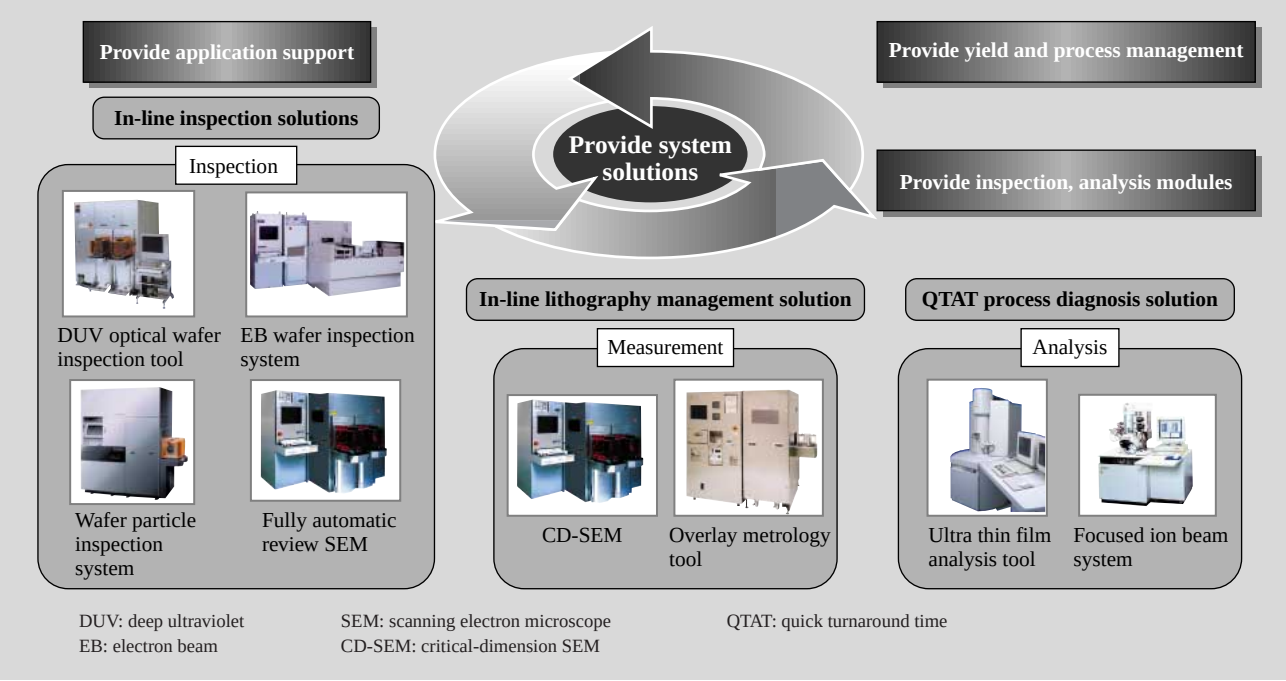

Fig. 1—Hitachi Group's Semiconductor Device Metrology, Inspection and Analysis Systems.
The Hitachi Group offers a wide range of stand-alone measurement, inspection, and analysis tools to aid in the efficient production of high-quality semiconductor devices. At the same time, the Group is building comprehensive management systems by organically combining these tools as integrated modules.

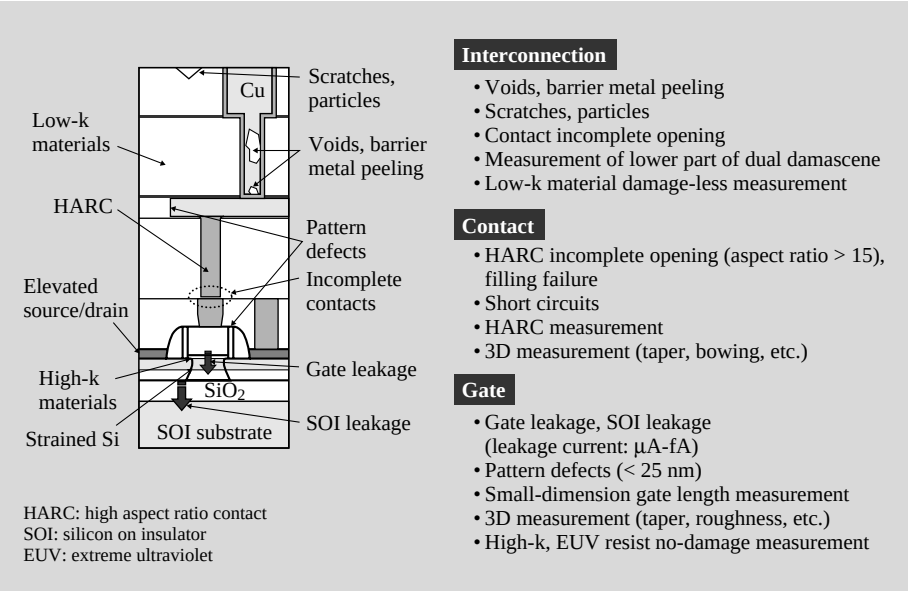

Fig. 2—Demands Raised by Semiconductor Devices. Types of device structures and defects expected in 90-nm-node semiconductor devices. We expect to see an increase in new low-k and high-k materials, and a range of new issues pertaining to defects and metrology.

short time frame, then working to enhance the device yield (including quality and reliability) as quickly as possible after the fab is up and running. A number of technologies are critically important in this process: technologies for in-line assessment of device patterns based on device design data, technologies for verifying faults, and technologies for evaluating the electrical characteristics of devices and for verifying the completed level of the final fine structure.

A variety of different measurement technologies are clearly required to analyze fine device structures, and it is important that these technologies are integrated in a comprehensive system in order to optimally position the right inspection and measurement tools, to efficiently extract the data that is needed, and to identify the fine geometry region that is targeted for analysis.

This article presents an overview of the Hitachi Group's IC (integrated circuit) inspection and analysis solutions that meet the increasingly diverse needs of chip manufacturers in supporting high-quality streamlined production of semiconductor devices (see Fig. 1).

REQUIREMENTS BASED ON SEMICONDUCTOR DEVICES

Fig. 2 shows some of the typical types of defects that cause problems in semiconductor device structures.

Basic trends today in designing device structures are to adopt strained Si, elevated source/drains, and SOI with the goals of increasing the operating speed of devices while inhibiting punch-through and reducing power consumption. We are also seeing increasing use of a diverse range new materials such as high-k materials for gate dielectrics and low-k materials for interlevel dielectrics.

Anticipating the types of faults that are likely to occur with these structures and materials, the primary areas calling for measurement and inspection include the dimensions and cross-section profile of the MOS (metal-oxide semiconductor) region, dopant profiles, and leakage current. Measurement and inspection tools that can effectively identify and quantify the types of problems encountered in the new low-k and high-k materials are in high demand including defects relating to film quality and thickness, shape of trenches for damascene interconnects, misshapen and incomplete high-aspect-ratio interconnects, pattern defects, particles, scratches, voids, and barrier metal peeling.

INSPECTION AND ANALYSIS SYSTEM LINEUP

The Hitachi Group has assembled a powerful set of metrology tools including a CD-SEM, a precision overlay metrology tool, and an AFM (atomic-force microscope). On top of that, Hitachi's inspection tools include an optical wafer inspection tool, wafer particle inspection system, an EB wafer inspection system, and a fully automatic review SEM system. Finally, Hitachi has also developed a system that collects and analyzes the data from these various tools and a sampling system that efficiently extracts just enough defect data from a huge number of defects to devise effective

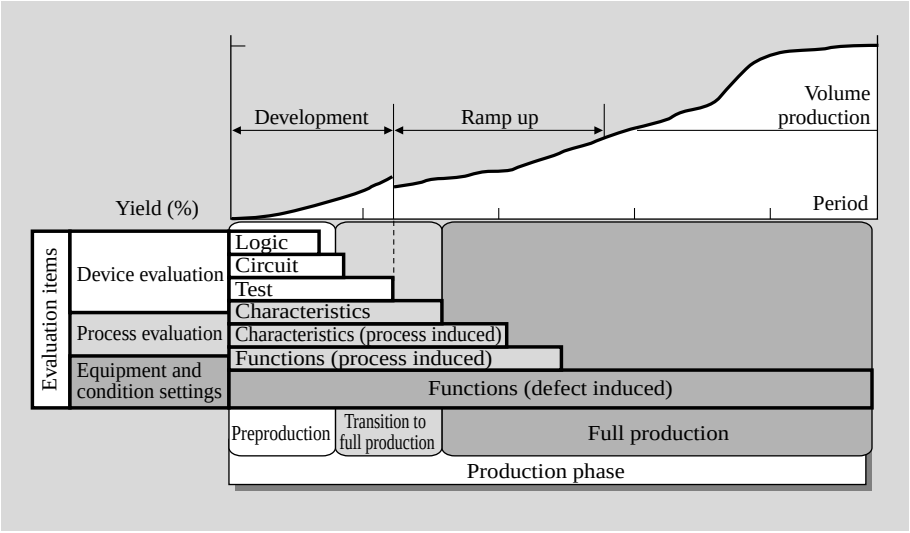

Fig. 3—Device Production Stage and Items for Evaluation.
Items for evaluation differ for different production stages. At the development and preproduction stage, evaluation of devices is the central concern. In the full production stage, dealing with particles and defects based on evaluation of equipment and condition setting becomes the central concern.

countermeasures. Obviously it is essential that these various metrology and inspection tools properly interwork based on sound operating guidelines and principles.

A whole different set of tools has been developed to evaluate and analyze device structures including an FIB (focused-ion-beam) system, a SEM, and an STEM. Here again, a sampling system is critically important to collect a relatively small but sufficient number of samples to make the correct structural assessment of a device. E-sampling (effective sampling) is also required in analyzing the vast number of defects that are detected by the inspection tools.

INSPECTION AND ANALYSIS SOLUTIONS

Yield Enhancement Initiatives

The primary objectives of any foundry fab are to maximize the wafer yield as early in the run as possible and to maintain the availability factor of the fab equipment at as high a level as possible. Critical in achieving these goals are the careful evaluation of devices and processes at the development/preproduction stage when the production process and equipment conditions (including margins) are set while debugging is in progress. Then, when ramping up to full production, the foundry fab processes and equipment are debugged based on comparison with the trial production results and the process and equipment condition settings. Particularly fabs involving very large investments are subjected to careful measurement and diagnostic evaluation to ensure that the equipment is used at maximum operating efficiency (see Fig. 3). If these evaluations are to be done efficiently, then the various component tools — CD-SEM and other metrology tools, optical wafer and other inspection tools, data collection and analysis systems, SEM, TEM (transmission electron microscope) and other analytical tools — must interwork smoothly as a total comprehensive inspection and analysis system. While making full use of this system, it is also important that it provides a comprehensive inspection and analysis solution that meets the needs of the new SoC (system-on-chip) era and supports the diverse requirements of the different device manufacturers.

Device Evaluation

Devices and process are subjected to close evaluation during the development/preproduction stage. The characteristics of a device are largely determined by the design and process implementing the device, so devices are evaluated by electrical testing after the device is completed. Assuming a problem in the current-voltage characteristics of a device, for example, if we are able to measure distribution of impurity elements in an actual device, then we can reassess the ion implant and other process conditions and come up with a sound solution to the problem. The STEM system shown in Fig. 4 includes an EDX (energy-dispersive X-ray spectroscopy) system that performs precision elemental analysis while correcting for time drift. Fig. 5 illustrates the use of this function to measure a distribution of $10^{20}/cm^3$ atoms of As (arsenic) in an actual device. Note that the actual measured results correlate very closely with the simulation results[4].

The same system can also determine the internal stress distribution state of a material by measuring the

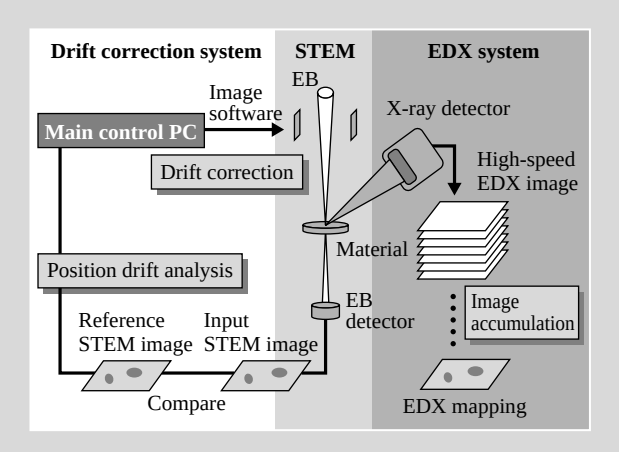

Fig. 4—EDX with Drift Correction Function.
High-sensitivity elemental analysis is performed through image accumulation while correcting the position.

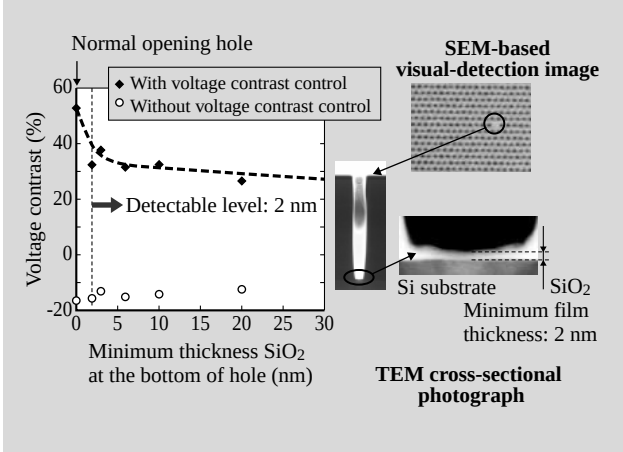

Fig. 6—Example of Residue Detected in Bottom of Contact Hole.
2 nm of SiO_2 residue is detected in the bottom of a high-aspect-ratio contact hole based on the voltage contrast.

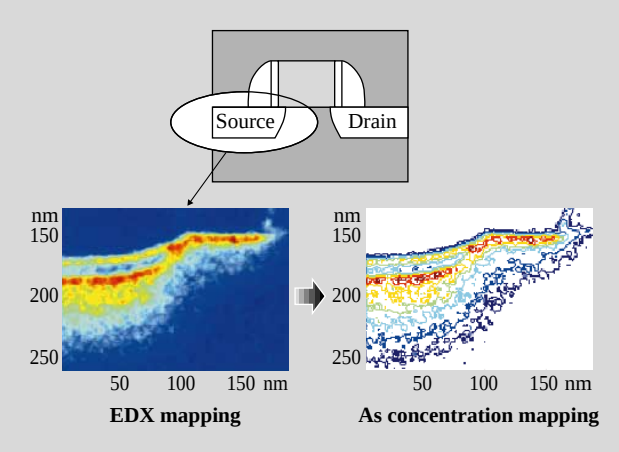

Fig. 5—Example of As Concentration Mapping.
Example shows a concentration map of As based on EDX mapping data of the transistor source area.

crystal lattice strain, so this tool should also be useful for measuring strained silicon[5]. And going beyond ordinary surface analysis, the STEM system is also capable of observing 3D structures using several-μm^2 micro-pillar samples, making the system useful for examining and analyzing even smaller device dimensions.

Use of these various kinds of analytical data not only improves the efficiency of device manufacture, it also contributes to much improved quality of devices.

Defect Detection

Devising ways to prevent the functional failure of devices caused by defects is the primary concern of the initial stage when ramping up to full production. In this defect detection process, optical wafer inspection and particle inspection tools are essential for detecting surface abnormalities such as scratches, particles, and pattern defects. There is also a variety of faults that cannot be readily observed from the surface such as voids, barrier metal peeling, and electrical defects, and EB wafer inspection tools are indispensable for spotting these kinds of defects[7]. These two different types of tools — those that examine the surface of devices and those that examine the interior of devices — complement each other and must be used together.

The principle of the EB inspection tool is called voltage contrast detection: an EB is directed at the surface of the wafer, and the emitted secondary electrons are detected. The amount of secondary electrons given off varies depending on the state of interconnects buried in the device (i.e., whether the interconnects are complete or not), and this shows up as contrasting images on the screen[8]. The beauty of this approach is that the detection sensitivity and detection object can be controlled by adjusting the voltage potential on the wafer surface. As shown in Fig. 6, this means that you can detect approximately 2-nm thick SiO_2 residue at the bottom of high-aspect-ratio contact holes by using negative-charge mode. This approach is also very effective at detecting internal short circuits and current leaks, and can therefore expose internal electrical problems that cannot be discerned from the surface. Fig. 7 shows an actual example of a leakage fault that was detected using this tool. Utilizing circuit design data and knowing how that data interrelates to detection conditions, we should

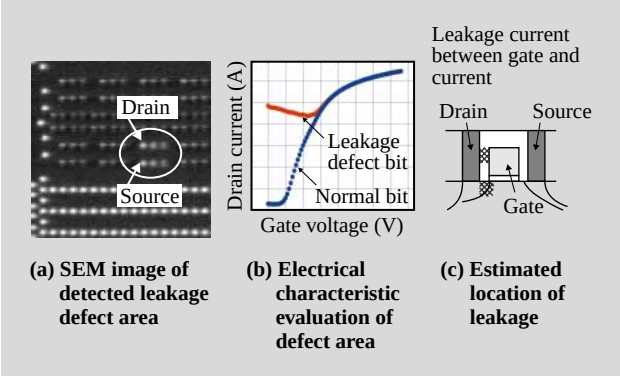

Fig. 7—Example of Leakage Defect Detection.
Leakage path is estimated in this example of an actual device by inspecting leakage defect detection results with an EB wafer inspection system based on measurements of electrical characteristics.

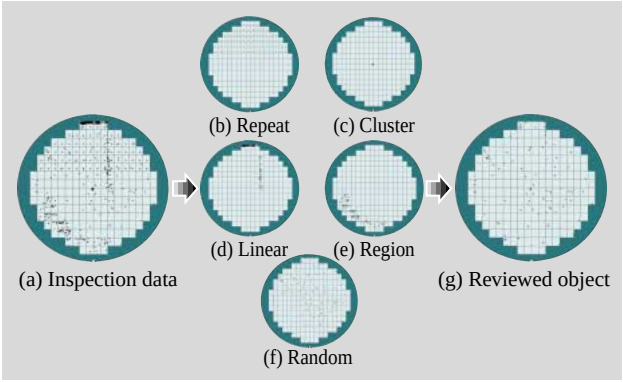

Fig. 8—Example of Defect Sampling by E-sampling.
E-sampling (effective sampling) functions can be used to sample review-targeted defects with high statistical reliability.

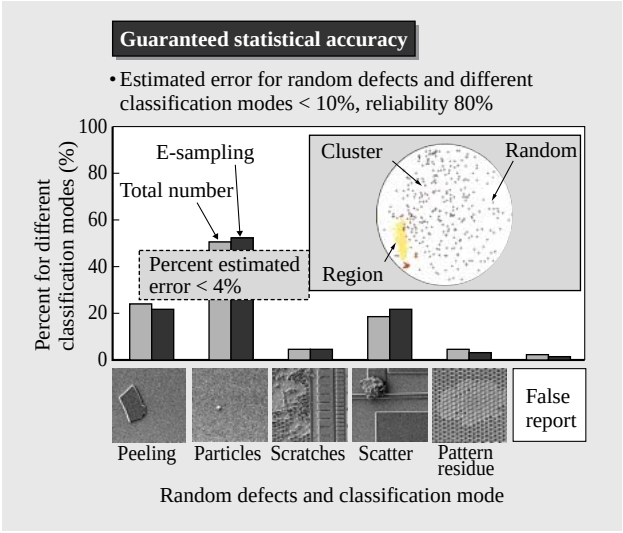

Fig. 9—Example of Data Showing Effectiveness of E-sampling.
The error is less than 10% and reliability greater than 80% for 86 sampling points out of a total of 2,647 defects (actual result when all points are reviewed is 4%).

in a few years be able to characterize the types of internals defects and their causes almost immediately.

Defect Review

Defect review involves a process of examining the particulars of faults based on the fault location data obtained by the inspection tools so the faults can be properly classified. A range of different kinds of faults occur in the development/preproduction stage, so it is important to identify and review the specific points that need to be analyzed[9]. As shown in Fig. 8, the E-sampling function of Hitachi's review support system generates a reliable statistical sampling of defects broken out by type and by frequency of occurrence[10, 11]. Fig. 9 illustrates the essential soundness of the E-sampling data. As shown in the figure that based on a sampling of only 86 defects (approximately 3.25% of 2,647 total defects), we obtain virtually the same results as when all of the faults are reviewed.

In addition to the voltage contrast faults, the EB wafer inspection system also detects ordinary pattern abnormalities and particles. In cases where priority measures are needed to prevent voltage contrast faults, the fully automatic review SEM is used just to identify the voltage contrast defects. With the EB wafer inspection system, a high-powered beam up to 100 nA is used because a high signal-to-noise ratio image must be obtained in a single scan. The problem is that this makes it impossible to recheck for voltage contrast faults using an ordinary SEM. This is solved by the review SEM system, which features a voltage contrast control electrode that enhances the system's ability to observe voltage contrast defects for an effective review[12].

When the primary objective of the review is to identify particles, a particle spectral analysis is performed using an EDX that is mounted on the review SEM system. In most cases, the EDX employs a high acceleration voltage of 15 kV because the goal is to perform a spectral analysis of all the elements. The problem is that at this high voltage the electrons penetrate deep into the wafer surface, so the signals from background patterns are counted. This diminishes the spatial resolution by as much as 3 μm which makes it impossible to characterize particle elements on product wafers. Here again, the review SEM system provides an effective solution. Using an acceleration

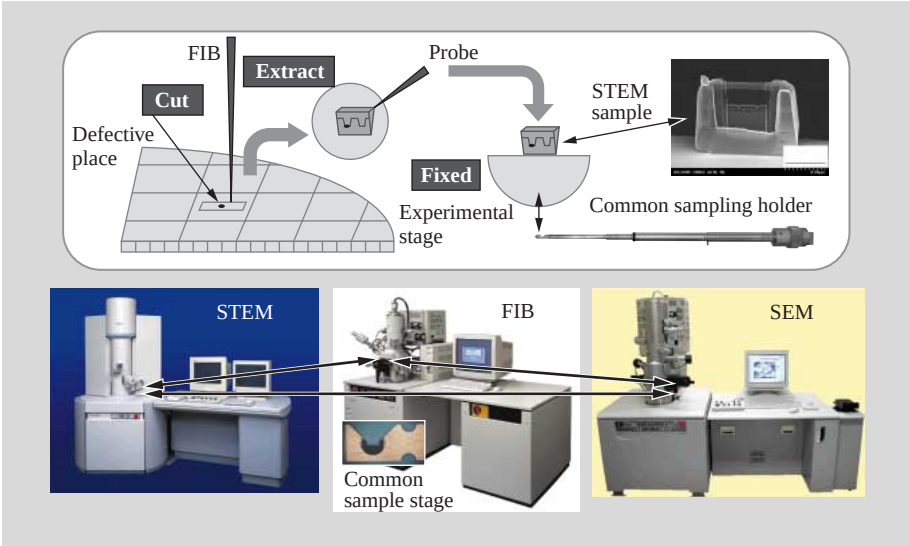

Fig. 10—Micro-sampling. The sample exposed to the FIB is attached to a probe and mounted on an experimental stage for observation. This permits high-resolution observation of the specific region in a short period of time.

voltage of only 5 kV, the spatial resolution is enhanced by about 0.7 μm so the particle elements on product wafers can be analyzed. Rather than the relative uncertainty of elemental identification using X-rays that are not sufficiently excited by 5 kV, we found that the spectrum pattern matching method is quite effective[13].

Defect Analysis

Ultimately, analysis by high-resolution SEM or TEM is required to determine the causes of defects that cannot be observed on the surface of devices. Any of a number of techniques might be used — taking multiple samples from around the area where the fault is located, extracting samples in different directions from which dies are marked out, etc.[14] — and the micro-sampling method has proved quite effective (see Fig. 10).

Fig. 11 shows how all of the tools and procedures outlined in this paper complement one another in a coherent flow from defect detection to defect review to defect analysis to first identify an incomplete contact failure in via hole of a copper damascene interconnect and then remedy the problem. A sequential system check is performed in which

(1) the EB wafer inspection system detects the incomplete contact failure in the via hole,

(2) the fully automatic review SEM uses E-sampling to verify the detected findings,

(3) the micro-sampling function of the focused ion beam system takes samples of the defect region, and

(4) the STEM system allows close observation of the device. In this actual product example, we were able

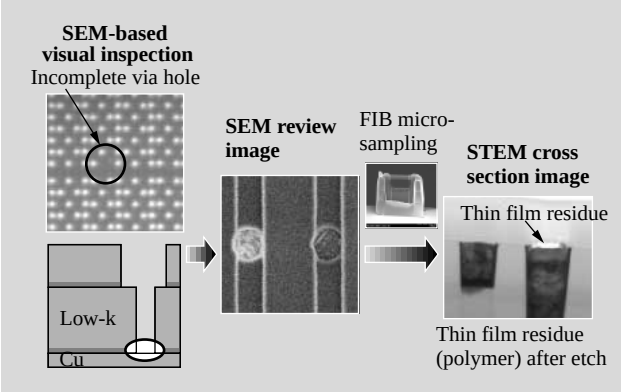

Fig. 11—Example of Transition from Fault Detection of Specification of Cause (Cu damascene).
A region of Cu damascene incomplete contact defects detected by the EB wafer inspection system is subjected to SEM review. Based on observation results of a cross-section defined by the micro-sampling method, the problem is traced to the etching.

to quickly isolate the problem within just a few days time and trace the source of trouble to polymer residue that built up when etching the low-k dielectric material. We also found that using an interconnect TEG (test element group) was an effective procedure for evaluating the QTAT of interconnect processes.

Data Analysis

The ability to access and manipulate various kinds of data are essential for the efficient production of high-quality devices. The range of different kinds of data include quality-related data: pattern dimension, overlay accuracy, and other kinds of measurement data; fault data; device characteristic data; and device testing data.

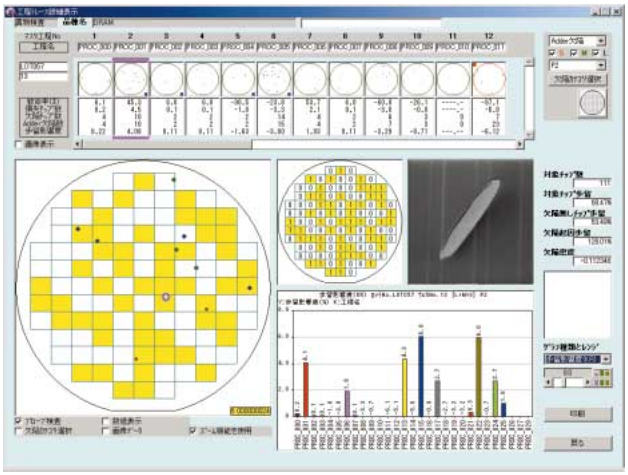

Fig. 12—Typical Calculation Showing Real-time Impact of Visual Defects on Yield.
Exploiting the data warehouse capability of the yield control system, the visual defects for each inspection process and their impact on yield can be derived in real time.

Beside quality-related data, there is also WIP (work-in-process) data that preserves a record of when, which tools, and which chambers were involved in the processing of each batch of devices. Hitachi's dedicated system is designed specifically to collect and analyze these various kinds of data. Especially noteworthy is the system's ability to perform a number of correlation analyses at high speed. A typical example is the "trace report function" illustrated in Fig. 12 that first characterizes the incidence of defects by comparing the occurrence of visual defects with the inspection results for each layer, then correlates those results with device characteristic data and electrical test results in real time. This capability is made possible by adopting a data warehouse[16] scheme in which much of the preprocessing that is required for the analysis is done in advance in real time. In the coming years, this kind of process analysis will require more detailed data including the temperature, type of gas, flow velocity, and other conditions under which semiconductor devices are produced. The next version system will feature data mining that extracts only the specific data needed from all this vast data, further promotes data warehousing to accelerate various processes, and functions that are tailored to users' needs.

CONCLUSIONS

This article surveyed some of the Hitachi Group's solutions for supporting high-quality, high-efficiency production of semiconductor devices.

While efforts to enhance yields were the central concern during the period of mass production of memories and other general-purpose products, the emphasis today with the strong prevailing trend toward SoC and small-lot large-variety production has shifted to the flow from inspection and metrology to analysis at the development and preproduction stage. Indeed, streamlining this flow offers an efficient way to enhance yields in the shortest time. Devising more advanced yield enhancing methods that are linked to semiconductor device design data are fundamentally important in this effort. For example, the ability to estimate device characteristics and the incidence of defects through simulation, and then perform inspections and measurements based on the estimates is required.

While certainly technologies enabling us to identify fault locations are extremely important from the standpoint of fault analysis, with present-day technologies it is still extremely difficult to pin-point exactly which transistor among several is the source of a problem even though we can identify which memory cell of an SRAM (static random access memory) is faulty. What we need to solve this dilemma is a technology enabling us to measure the electrical characteristics of individual transistors. The availability of this technology would certainly contribute to more reliable semiconductor devices.

We have seen a lot of diversification in the products of different device manufacturers in recent years, and this of course means that the need for yield enhancement measures has also become more diversified. It is no longer enough to just offer a uniform set of systems and tools. Rather, we must develop a clear understanding of our diverse clients' needs, then provide solutions that are tailored to those needs. This is the goal that the Hitachi Group has set for itself.

REFERENCES

(1) International Technology Roadmap for Semiconductors 2002 Update.
(2) N. Yanagiya et al., "CMOS Technology (CMOS5) with High Density Embedded Memories for Broadband Microprocessor Applications," Proceedings of IEDM 2002 (Dec. 2002).
(3) T. Noguchi et al., "65 nm Process Technology with Embedded DRAM Debuts," Nikkei Microdevices (Jan. 2003) in Japanese.
(4) R. Tsuneta et al., "A Specimen-Drift-Free EDX Mapping System in a STEM for Observing Two-Dimensional Profiles

of Low Dose Elements in Fine Semiconductor Devices," Journal of Electron Microscopy (Mar. 2002).
(5) M. Koguchi et al., "High-Resolution Stress Mapping of 100 nm Devices Measured by Stress TEM," Proceedings of SSDM 2001 (Sep. 2001).
(6) M. Konno et al., "FIB Micro-Pillar Sampling Technique for Three Dimensional Characterization," LSI Testing Symposium 2002 (Nov. 2002) in Japanese.
(7) M. Tanaka et al., "Detection Threshold Optimization and Application to In-line SEM Inspection," International Symposium on Semiconductor Manufacturing 2002 Conference Proceedings (Oct. 2002).
(8) M. Nozoe et al., "Analytical Technology for Deep Sub-Micron Process (2), Analysis of Contact Hole Failure using Voltage Contrast Image," Proceedings of the 46th JSAP annual meeting (Mar. 1999) in Japanese.
(9) N. Eguchi et al., "Semiconductor Yield Enhancement Solution for Next Generation," Hitachi Hyoron **84**, pp.261-266 (Mar. 2002) in Japanese.
(10) Y. Takagi et al., "Visual Pattern Detection of Spatial Point Set," Technical Report of the Institute of Electronics, Information and Communication Engineers (Jun. 2001) in Japanese.
(11) Y. Takagi et al., "Defect Monitor Method Based on Sampling Review Plan," Proceedings of The Japan Society for Precision Engineering "Visual Inspection Workshop" (Dec. 2001) in Japanese.
(12) K. Watanabe et al., "Efficient Killer-Defect Control Using Reliable High-Throughput SEM-ADC," The 12th Annual IEEE/SEMI Advanced Semiconductor Manufacturing Conference (Apr. 2001).
(13) I. Ochiai et al., "Recognition of Elements and Materials with Sub-micron Resolution by X-ray Analysis for Review SEM," LSI Testing Symposium 2002 (Nov. 2002) in Japanese.
(14) M. Furuta et al., "TEM Analysis Technique for the Electric Current Leakage Failure Caused by Crystal Defect," LSI Testing Symposium 2002 (Nov. 2002) in Japanese.
(15) K. Umemura et al., "Development of 'Micro-sampling Technique' for Transmission Electron Microscope," Journal of The Japan Society for Precision Engineering **68**, No. 6 (Jun. 2002) in Japanese.
(16) H. Iwata et al., "In-line Wafer Inspection Data Warehouse for Automated Defect Limited Yield Analysis," The 11th Annual IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop (Sep. 2000).

ABOUT THE AUTHORS

Kenji Watanabe

Joined Hitachi, Ltd. in 1978, and now works at the Application Technology Department, Semiconductor Process Control Systems Sales Division, Device Manufacturing Systems Business Group of Hitachi High-Technologies Corporation. He is currently engaged in the development of LSI inspection and application analysis technologies. Dr. Watanabe is a member of the Japan Society for Precision Engineering, and can be reached by e-mail at watanabe-kenji@naka.hitachi-hitec.com.

Aritoshi Sugimoto

Joined Hitachi, Ltd. in 1979, and now works at the Application Technology Department, Semiconductor Process Control Systems Sales Division, Device Manufacturing Systems Business Group of Hitachi High-Technologies Corporation. He is currently engaged in the development of LSI inspection and application analysis technologies. Mr. Sugimoto is a member of The Japan Society of Applied Physics (JSAP) and The Institute of Electrical Engineers, Inc. (IEEE), and can be reached by e-mail at sugimoto-aritoshi@nst.hitachi-hitec.com.

Mari Nozoe

Joined Hitachi, Ltd. in 1986, and now works at the Advanced Technologies Development Department, the Solutions LSI Development Center of Central Research Laboratory. She is currently engaged in the development of EB-based semiconductor inspection and analysis technologies. Ms. Nozoe is a member of JSAP and IEEE, and can be reached by e-mail at mnozoe@crl.hitachi.co.jp.