New Semiconductor Device Evaluation System for Failure Analysis of Sub-nanometer Areas

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OVERVIEW: Increasingly higher circuit integration, density, functionality, and reliability of semiconductor devices demand a higher spatial resolution and user-friendliness for TEMs (transmission electron microscopes) and SEMs (scanning electron microscopes) that are used for failure analyses and other observation purposes. In response to these requirements, Hitachi Group has developed a new semiconductor device evaluation system by integrating a focused ion beam system and an ultra-thin film evaluation system based on STEM (scanning transmission electron microscope). For the best compatibility of rapid sample milling and fine milling conditions, the focusing ion beam system has an accelerating voltage range of 10 to 40 kV. The ultra-thin film evaluation system has both bright and dark field STEM detectors as well as a secondary electron detector for observing and obtaining a versatile specimen structure and compositional information. For analytical applications, it can also be used with an energy dispersive X-ray spectrometer and an electron energy-loss spectrometer. By making use of these detector/spectrometer systems, the ultra-thin film evaluation system can observe fine atomic-level structures and it can map light elements of sub-nanometer areas in real-time. In addition, we have developed a compatible specimen holder, which can be used with both the focusing ion beam system and the ultra-thin evaluation system without repositioning the sample. Furthermore, we have developed a micro-sampling technique that enables preparing site-specific specimens of any particular point from a device sample. With this technique micro-samples can be prepared with a positional accuracy of 100 nm or higher and the samples can be evaluated in four to five hours.

INTRODUCTION

FOR the evaluation of semiconductor devices, probes of various charged particles have been used. All techniques used in the evaluations take advantage of interactions between the charged particles and samples. Due to the characteristics of these interactions, the given information, such as sample structures, compositions, and chemical bonding, differ from one technique to another. Light optical observations, for example, have been used to search for foreign particles within the crystals of substrate materials. Spectroscopy using high energy ions or X-rays is an effective method for evaluating heterogeneous boundaries of metals. Spectroscopy using secondary ions has been applied to analyze fine impurities. Raman spectroscopy using a laser beam has been applied to stress-analyses in materials.

When it comes to spatial resolution, however, most of these techniques are limited to sub-microns or a few microns due to their operating principles. For structure analyses in the sub-nanometer range, therefore, SEMs and TEMs have been extensively used. TEMs are one of the few instruments that achieve a high resolution microscopy at atomic scale. They are promising instruments for 100-nm process evaluations. Using TEMs, however, requires experience and skill, so an equally high-resolution instrument that is easier to use is being sought after. In addition, site-specific sample preparations are required for failure analyses. High-resolution TEM is an important technique for evaluating structures. Conventional focused ion beam techniques enable sample preparations for TEM but the available positional accuracy from the specific area of interest

Fig. 1—Semiconductor Device Evaluation System is Composed of Focused Ion Beam System (a) and Ultra-thin Film Evaluation System (b). This evaluation system utilizes the 40-kV and the 200-kV accelerating voltages of the focused ion beam system and the ultra-thin film evaluation system, respectively, and it completes failure analyses of semiconductor devices and structure analyses of sub-nanometer areas within a few hours.

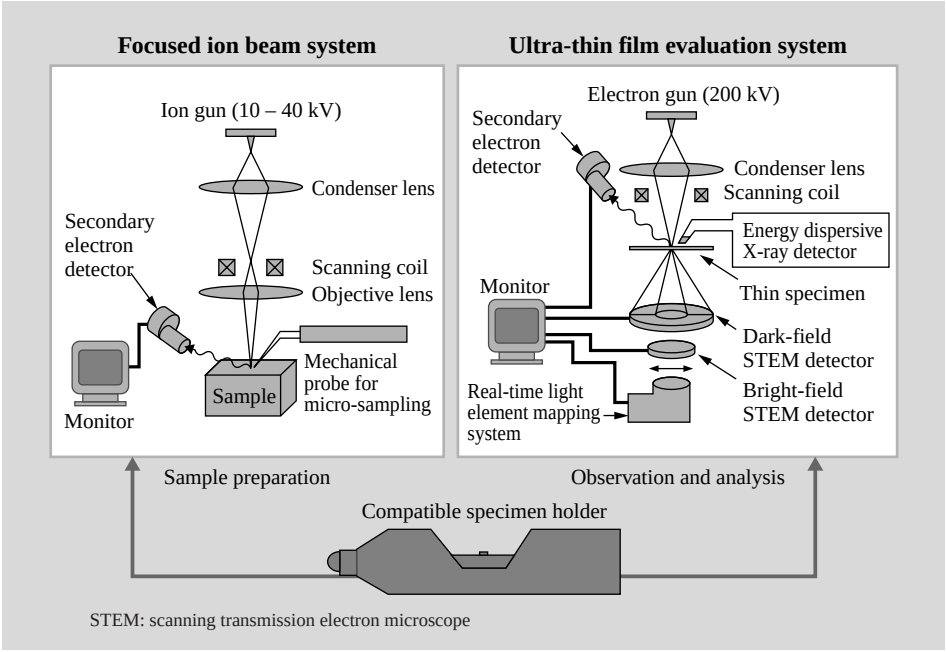

Fig. 2—Configuration of Semiconductor Evaluation System: Integration of Focused Ion Beam System and Ultra-thin Film Evaluation System. This semiconductor evaluation system is applicable to devices with 100-nm processes, and it uses a compatible specimen holder for sample preparations and analyses of structures and compositions.

is approximately 200 to 300 nm. These techniques are difficult for thin sample preparations that require a positional accuracy with a maximum allowable deviation of 100 nm.

We describe the functions, features, and some applications of the new semiconductor device evaluation system we have developed in the Hitachi Group.

OPERATING THEORY AND CONFIGURATION OF SEMICONDUCTOR DEVICE EVALUATION SYSTEM

To prepare a thin sample of a specific area of failure from a semiconductor device, we need to know the position of the failure. A common technique is to observe a sample during the milling process by using an SIM (scanning ion microscope) image of a focused ion beam system. Since this technique uses an ion beam to scan probes, the sample is damaged by the ion beam illumination. To resolve this problem, we have combined a focused ion beam system and an ultra-thin film evaluation system (see Fig. 1).

The semiconductor device evaluation system is shown in Fig. 2. We used a focused ion beam system[1)] for the sample preparation. For observing the prepared sample, we used an ultra-thin film evaluation system[2)]. The focused ion beam system operates at a 10- to 40-kV accelerating voltage. The higher voltage enables rapidly milling samples and the lower voltage obtains a clean surface finish. By selecting the optimum accelerating voltage, a clean and thin sample can be prepared.

For preparing a small sample piece called a micro-sample, we have developed a mechanical probe[3)]

which enables directly extracting the micro-sample from bulkier samples. In a mechanical probe operation, the SIM image is highly magnified so inexperienced operators can pick up the micro-samples without fail. Using a precision cutter to cutout a sample is no longer required.

We used a cold field emission electron source for the ultra-thin film evaluation system for operations at 200 kV. This allows clear inner-structure images of silicon devices that are a few microns thick. The probe of this instrument is minimum approximately 0.2 nm large and it enables high resolution STEM image observations of atomic-scale materials. For a maximum acquisition of sample information such as structures, compositions, and chemical bonding conditions, we have incorporated both bright- and dark-field STEM detectors and a secondary electron detector.

For analytical applications, we have incorporated an energy dispersive X-ray detector and a real-time light element mapping system. Hitachi developed a compatible specimen holder for use with focused ion beams and ultra-thin film evaluation systems. It allows repeated ion milling and observations without having to reposition the sample once it is mounted on the holder.

The semiconductor evaluation system we developed permits site-specific thin specimen preparation at a positional accuracy of 100 nm or higher, structure analysis of sub-nanometer areas and smaller, elemental analysis of compositions, and the analysis of chemical bonding information.

SAMPLE PREPARATION AND OBSERVATION

Micro-sampling Technique to Directly Cutout Samples from Specific Area of Interest in FIB System

Fig. 3 shows the sequence of a micro-sample preparation using the focused ion beam system. First, the sample is protected, specifically the area of interest (shown by an arrow), by metal deposition (a). This sample protection is important since the sample may be damaged or contaminated by a focused ion beam during the preparation. Then, one or several grooves are made around the area of interest (b). The sample is tilted and the bottom of the area of interest is milled (c). Next, the mechanical probe is moved so the tip makes contact with a corner of the area of interest and it is bonded together by metal deposition (d). Then, the micro-bridge supporting the area of interest is cutoff by ion milling and the micro-sample is picked up (e). The micro-sample is typically 10 to 15 μm wide, 3 to 5 μm thick, and 10 to 15 μm high. Preparation typically takes approximately one hour.

Fig. 4 shows a micro-sample prepared from an Si device. The specimen was prepared in the form of a pillar at about 5 μm^2 and was mounted on a corn shaped sample stub. With this arrangement, the pillar sample can be viewed at all orientations, and hit also facilitates

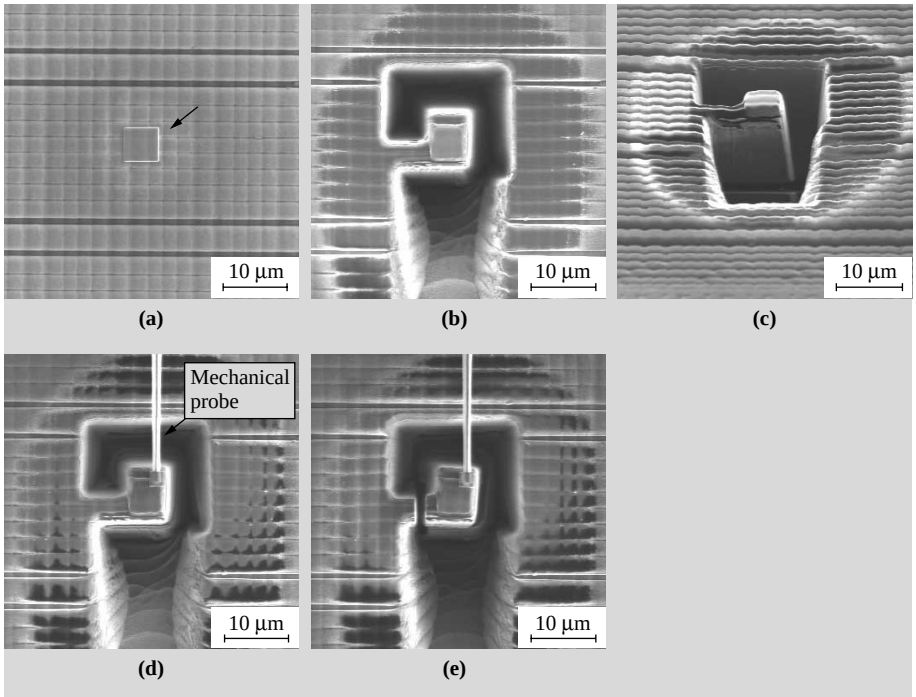

Fig. 3—Sequence of Micro-sample Preparation.
The area of interest on a semiconductor device has been prepared. Scanning with a focused ion beam creates various sample shapes.

cross-sectional observation. It allows a quick view of specific failures of a location.

Observation of Micro-samples

STEM images are less susceptive to chromatic aberrations than TEM images. This STEM characteristic is advantageous for observing thick samples. The semiconductor device evaluation system allows searching for failures based on this sample imaging. Fig. 5 shows STEM and SE (secondary electron) images of an approximately 2-μm^2 pillar-shaped DRAM micro-sample observed at a 200-kV accelerating voltage. Both images were observed from the same direction but they both provide different structural information. The STEM image shows fine structures of the capacitors and the arrangements of upper and lower wirings. The SE image shows fine sectional structures of the capacitors, wiring and contacts viewed 3D (three dimensionally) and at two angles differing by 90 degrees. For a failure analysis, beginning with a thick sample observation is best. Then, additional milling and observation can be repeated in alternation until the final failure point is reached.

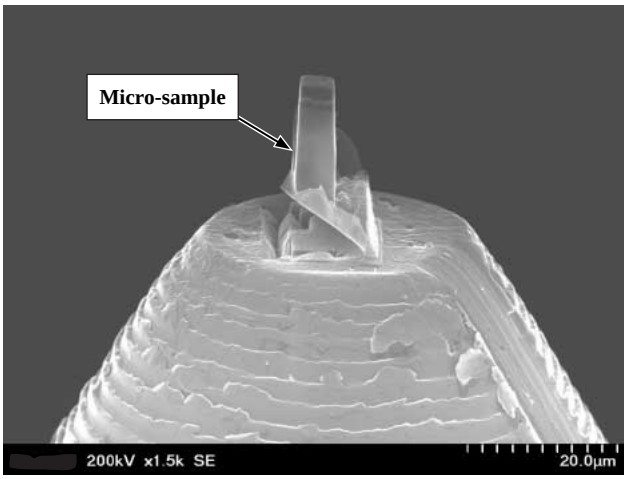

Fig. 4—5-μm^2 Pillar-shaped Micro-sample Prepared from DRAM (dynamic random access memory). By mounting the pillar sample on a corn shaped stub of the sample can be viewed and examined from all directions.

Searching Failures and Thinning Sample

When a failure is a feature of a sub-micron sized sample or smaller, we need to thin the sample without losing the failure and without damaging the sample with the ion beam irradiation. This is very difficult with normal focused ion beam techniques. Our system has been developed to meet these requirements. Fig. 6 shows our technique. When a failure point has been roughly determined as shown in Fig. 5, the sample thickness is reduced to approximately 3 to 5 μm [Fig. 6-(a)]. After milling, the sample is put in the ultra-thin film evaluation system and observed in the STEM [Fig. 6-(b)] and SE modes [Fig. 6-(c)] on both sides and the failure point is specified. The sample is then put back into the focused ion beam system and additional milling is conducted. The milling and observations are repeated until, finally, the sample thickness is reduced to 0.1 μm or less at the failure point [Fig. 5-(d)].

Fine Structure Observation of Thin Sample

Fig. 7 shows a high-resolution STEM image of a thin DRAM gate sample prepared as above. The sample was approximately 60-nm thick and it was observed at 200 kV. The EB (electron beam) was

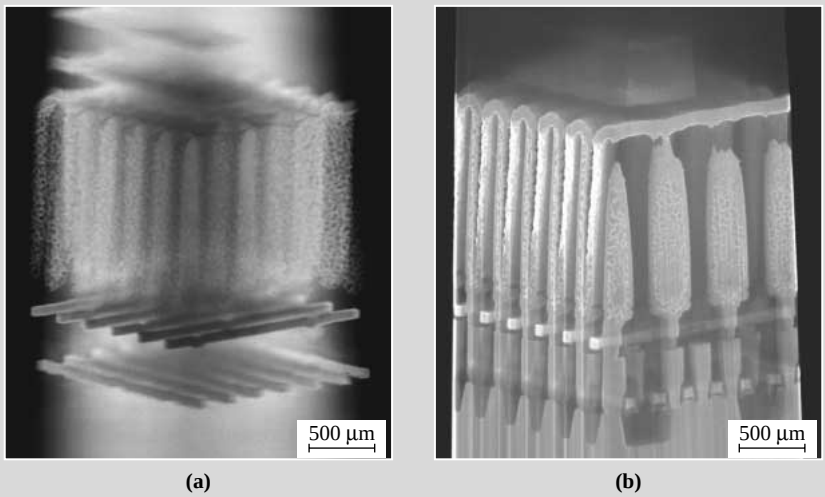

Fig. 5—STEM (a) and SE (b) Image of a 2-μm^2 Pillar-shaped DRAM Micro-sample. The STEM image (a) shows fine structures of the capacitors and arrangements of two stage wirings. The SE (b) image shows a sectional structure of capacitors viewed from two directions 90 degrees apart.

normal to the (110) plane of the Si-substrate crystal and the crystal lattice image of the Si (111) plane with a 0.314-nm lattice spacing was clearly observed. Another crystal lattice image showing similar spacing was also clearly observed at the gate area. Thin samples prepared by using focused ion beam systems generally suffer damage from the ion beams and using high-resolution microscopy is difficult. Our system, however, allows thin sample preparations without damaging.

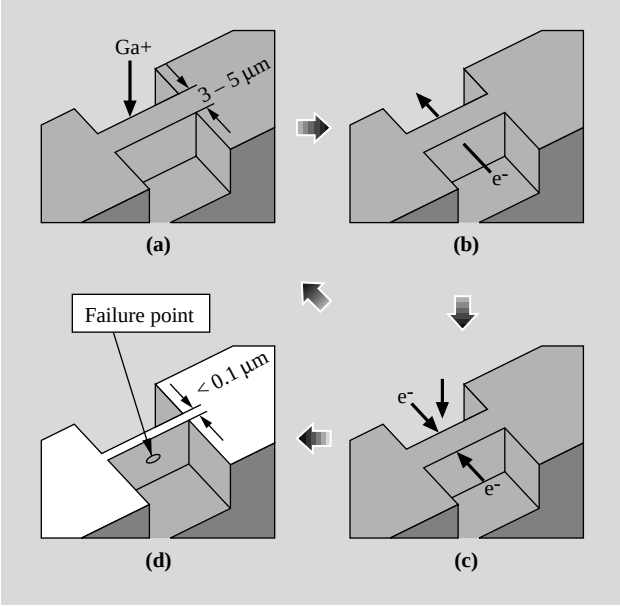

Fig. 6—Locating Failure Point and Thinning Sample. A sample prepared a few microns thick (a) is mounted on the STEM and analyzed for defects (b) and (c). After determining the failure point, the sample is put back into the focused ion beam system and milled. By repeating the milling and the observations, the sample thickness is reduced to 0.1 µm or less at the failure point (d).

Real-time Light Element Mapping

Analyzing of semiconductor devices requires evaluating the shapes and thicknesses of the insulation layers. To analyze the insulation layers, energy dispersive X-ray spectrometry or electron energy loss spectroscopy have been used. Recording an image with these spectrometers is time consuming; it usually takes up to about 30 minutes. To expedite the analysis, we have developed a real-time light element mapping system based on electron energy loss spectroscopy, as shown in Fig. 8. This system allows acquiring electron signals selected from an element of interest together with their background signals. It has two electron

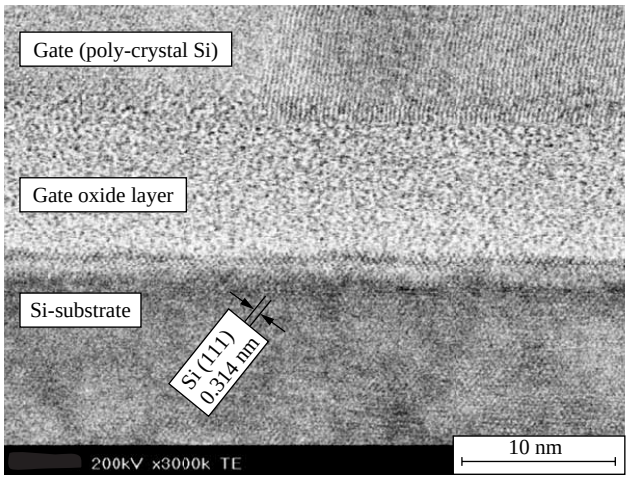

Fig. 7—High-resolution STEM Image of Thin Si-device Gate Area Prepared by Using Semiconductor Evaluation System. The sample has been thinned to about 60 nm. A 0.314-nm crystal lattice spacing can be seen clearly at Si (111) plane of the Si-substrate and gate area.

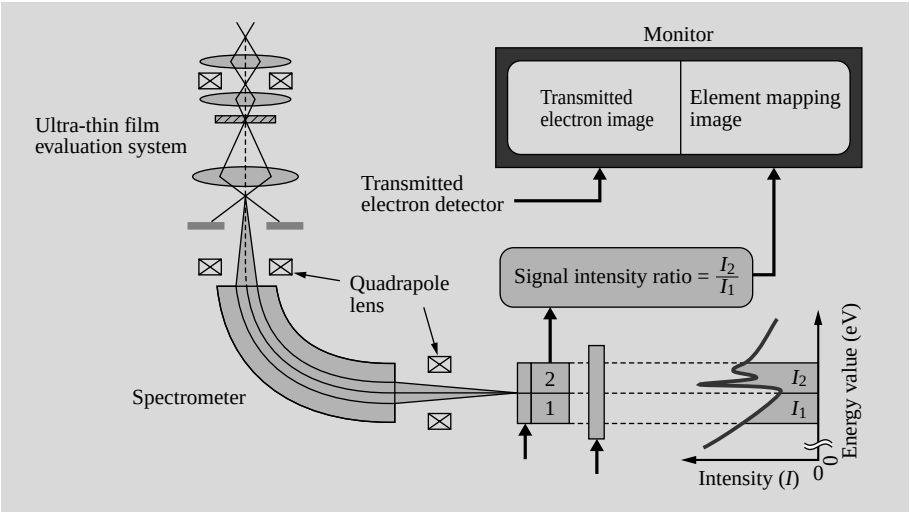

Fig. 8—Ray Diagram of Real-time Light Element Mapping System. Two detectors are positioned at the back of the spectrometer. This arrangement allows real-time light element mapping.

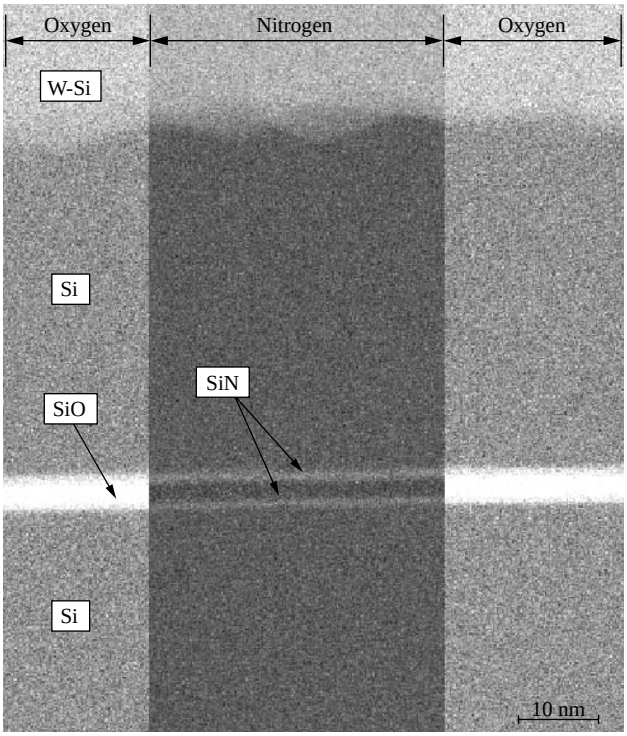

Fig. 9—Insulation Layer Recorded by Using Real-time Light Element Mapping System.
During the scanning operation of the primary EB, the mapping signals were changed from oxygen to nitrogen and back to oxygen again. The shapes and thicknesses of the SiO and SiN layers were clearly observed.

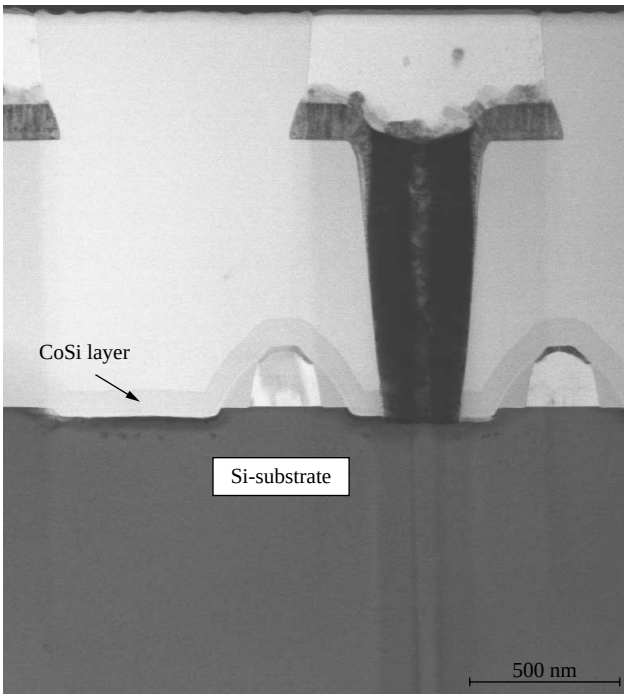

Fig. 10—Low Magnification Sectional View of SH-Microprocessor (Transmission Image).
The dark layer above the Si-substrate is the CoSi diffusion layer.

detectors at the back of the spectrometer. The intensity ratio of these signals (I_2/I_1) is converted to a signal intensity displayed on a monitor in a form of real-time light element mapping and in synchronism with the scanning EB. The system can map images in approximately 1/10 of the time needed with conventional spectrometers.

Observation of Insulation Layers

Fig. 9 shows an image of insulation layers in an Si-device recorded by using the real-time light element mapping system. In this observation, the acquired signals of the mapping images were changed from oxygen to nitrogen and back to oxygen again. The recorded image shows the shapes and thickness of the SiO, SiN, and SiO layers and their respective positions very clearly. It took us 80 seconds to record this mapping image.

APPLICATION TO PRACTICAL DEVICE ANALYSES

We have used the new semiconductor device evaluation system for evaluating fine structures of CoSi diffusion layers of a device used on an SH-microprocessor of Renesas Technology Corporation. Fig. 10 shows a low magnified sectional view of the CoSi diffusion layer and its surrounding area. The sample was approximately 0.5-μm thick. The cross-section of a W contact hole can be clearly observed. Fig. 11 shows a highly magnified image. An abnormal image contrast can be seen in the Si-substrate, just underneath the CoSi diffusion layer. We have thinned this sample to approximately 60 nm without destroying

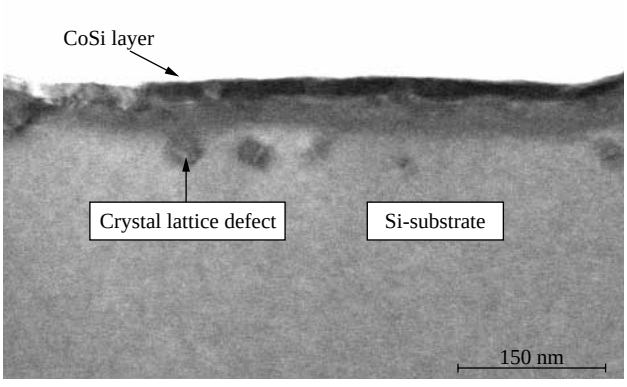

Fig. 11—Sectional STEM Image of CoSi Diffusion Layer, SH-Microprocessor.
An abnormal contrast appeared inside the Si-substrate below the CoSi diffusion layer.

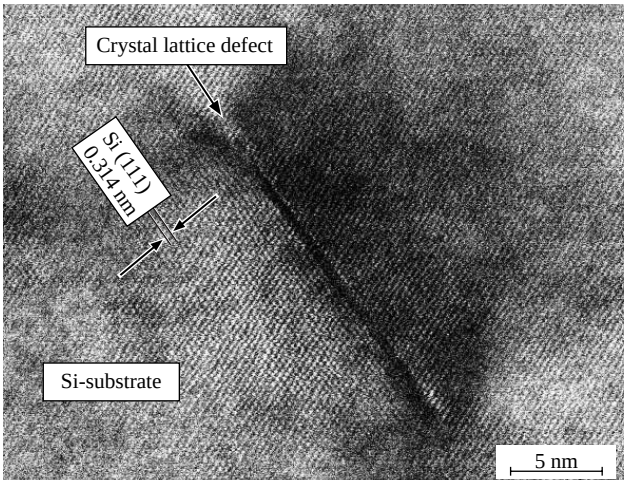

Fig. 12—Crystal Lattice Defect in Si-substrate below CoSi Diffusion Layer.
The defect is in the Si (111) plane and approximately 20-nm long.

the structure. Fig. 12 shows a highly magnified STEM image. It clearly shows a 0.314-nm crystal lattice spacing of Si (111). From this high resolution STEM observation, we concluded that the abnormal contrast below the CoSi diffusion layer was due to crystal lattice defects and that the approximately 20-nm long defect was in the Si (111) plane.

CONCLUSIONS

We have developed a semiconductor device evaluation system with an integrated focused ion beam system and an ultra-thin film evaluation system with its functions, features and some applications for failure analyses.

The system can prepare thin samples at a positional accuracy of 100 nm or higher from a specific area of interest and analyze atomic-level structures.

Hitachi Group aims at developing instruments and techniques compatible with processes at 100 nm and smaller to contribute to the advance in semiconductor device fabrications.

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