# UHF-ECR Plasma Etching System for Dielectric Films of Next-generation Semiconductor Devices

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OVERVIEW: As semiconductor device technology evolves with shrinking of feature dimensions, this is driving demand for dielectric film etchers supporting tight CD (critical dimension) control and stable processing. Particularly, as the era of 90-nm feature semiconductor devices fast approaches, the need for a dielectric etcher has emerged as a high-priority concern that will accommodate (1) HARC (high aspect ratio contact) control with an aspect ratio greater than 20, (2) tight CD control with ArF and hard mask etching for gates, and (3) low-k (dielectric constant of less than 2.5) materials for damascene processes. To address these needs, Hitachi Group has developed a dielectric etcher that uses UHF-ECR (ultra-high frequency electron cyclotron resonance) and achieve excellent plasma control. Able to accommodate 200- to 300-mm size wafers, the etcher can be applied to a broad range of etching processes including HARC, gate mask etching, damascene processing of organic and inorganic low-k materials. The favorable assessment of customers in how well the system meets their performance needs is reflected in the large number of orders for the system. The system has the same base frame as previous systems that already have a solid track record on quantity production fab lines, so excellent reliability is assured.

# INTRODUCTION

FINER featured semiconductor devices providing high levels of functionality and denser chip integration are indispensable for all the digital equipment and systems supporting the ubiquitous information society. Fabrication of these devices will require smaller geometry 100-nm structures and the adoption of new materials, and this is fueling a demand for new etching technologies that will support these smaller tolerances.

Processing of dielectric materials in particular involves a number of processing challenges including the processing of gate masks with a tight CD (critical dimension) control since this determines the transistor speed, processing of transistor contact holes with high aspect ratio to increase memory capacitance, and via hole and trench dual damascene processing of new low-k materials that are now starting to be used for interconnect interlayer dielectric layers<sup>1, 2)</sup>.

Hitachi Group has sought to accommodate these demands with the development of a UHF-ECR (ultrahigh frequency electron cyclotron resonance) etcher for next-generation processes (see Fig. 1). This article will give an overview of the etcher, highlighting the system's principle features, performance, and a number of process application examples.

# UHF-ECR PLASMA ETCHER'S FEATURES AND CONFIGURATION

Dielectric etching applications typically rely on the competing influences of polymer deposition and reactive ion etching caused by disassociated fluorocarbon gas species. This means that to achieve greater etching accuracy, it is necessary to impose tighter control over the dissociation species bombarding the wafer. Among these dissociated species, controlling the ratio of  $CF_2/F$  radicals affects the selectivity of the mask and the substrate and high aspect ratio hole openness. Control of the ion ratio to  $CF_2$  radicals is also important, for this affects the etching profile.

By achieving better control over these parameters, the UHF-ECR etcher is capable of etching finer features for the 90-nm technology node and beyond. Fig. 2 shows a schematic representation of the etching chamber for dielectric layers. Here we will highlight two main features of this approach:



Fig. 1—Appearance of UHF-ECR Dielectric Film Etcher of Next-generation Processes (a), and Processing Examples (b).

For HARC (deep hole) processing and Cu damascene processes, the interlayer dielectric film etcher provides excellent profile control and can accommodate 300-mm wafers at the 90-nm and 65-nm technology nodes.



Fig. 2—Schematic Representation of Etching Chamber. A stable medium density gas plasma is produced at low-tomedium gas pressure through interaction between UHF waves from a flat antenna and a magnetic field produced by a solenoid coil.

(1) The ECR plasma is formed by 450-MHz UHF waves and a magnetic field. This enables the formation of a medium-to-high density plasma at low-to-medium gas pressure that is required for fine feature processing. By using UHF band frequencies, fluorocarbon gas disassociation and production of excess F are suppressed<sup>3)</sup>. This effectively reconciles good selectivity of the mask with high aspect ratio processing.



Fig. 3—Principle of Plasma Distribution Control for Etcher. The distribution of plasma is controlled by using coil current to shift where high-density plasma is generated  $A \leftarrow B \rightarrow C$ .

In Fig. 3 one will also observe that the distribution of the plasma can be controlled by regulating the ECR surface by the magnetic coil current. This enables a uniform distribution of plasma across the entire surface of the wafer under various processing conditions. (2) The UHF waves are introduced to the chamber by a flat antenna, and there is a semi-narrow gap of 30 to 100 mm between the flat antenna and the wafer. As illustrated in Fig. 4, the radical ratio of the plasma can



Fig. 4—Control of Active Species in Plasma by Adjusting Gap. For narrow gap settings, mask selectivity is increased. For wide gap settings, good CD control and vertical profiles are obtained.

be regulated by varying the width of the gap. This configuration results in an ECR plasma zone beneath the antenna of about 20 to 30 mm and a diffusion plasma zone under the ECR plasma zone. The ECR plasma produces ions and relatively high concentrations of  $CF_2$  radicals, while the diffusion plasma zone produces relatively high concentrations of F radicals. Therefore, reducing the gap increases the  $CF_2/F$  ratio which increases selectivity of the resist, while increasing the gap does just the opposite: the  $CF_2/F$  ratio in deceased which produces a plasma supporting excellent CD and vertical sidewall control.

Using the UHF power to independently control the gap and the antenna bias and adjusting the ratio of  $CF_2$  to F radicals and ions to  $CF_2$ , the UHF-ECR etcher can be easily optimized to accommodate a wide range of processing applications including holes, masks, damascene, via holes, trenches, and more. Because the plasma is generated at some remote from the sidewalls, it has virtually no adverse effects on the sidewall materials.

# HARC ETCHING PROCESS

The basic requirements for HARC (high aspect ratio contact) etching process are summarized as follows:

(1) Assurance of good vertical profile

(2) High degree of selectivity for mask material (PR: photoresist)

(3) Good control over CD shift tolerances

In hole processing, balance among radicals dissociated from fluorocarbon gas is controlled on the  $CF_2/F$  rich side, and reconciling high aspect ratio hole openness, vertical profiles, and selectivity to masks and substrates are important<sup>4</sup>).



Fig. 5—Examples of 0.09-µm HARC Etching Process. Good vertical profile without bowing and resist selectivity are reconciled by processing with a narrow gap setting at low pressure.

Using the UHF-ECR etcher, the radicals dissociated from the fluorocarbon gas are controlled by reducing the gap between the antenna and wafer, and this increases the CF<sub>2</sub>/F ratio. Moreover, the reactivity between excess F and shower plating material Si is controlled by the antenna bias, and this enables the CF<sub>2</sub>/F ratio to be controlled. Good vertical profiles are easily achieved using the low-pressure region. Fig. 5 shows processing examples for a 0.1- $\mu$ m hole with an aspect ratio greater than 20.

### GATE MASK ETCHING PROCESS

As gate geometries diminish, the following are required to achieve the greater precision and dimension control over hard-mask etching for gates:

(1) Assurance of good vertical profile

(2) Good selectivity of substrate material (WSi, poly-Si) (3) Control over the CD shift amount

(4) Applicability to ArF resist mask with low plasma resistance

The principle objectives of mask etching are to ensure good vertical profiles for the BARC (bottom anti-reflection coating), the BARL (bottom antireflection layer), SiN, and TEOS (tetra-ethoxysilane) while imposing an appropriate degree of control over the CD shift. The etching profile and CD shift are largely determined by the etching rate in the vertical and horizontal directions with respect to the planar surface of the wafer, so it is important to achieve the right balance between the etchant component and the deposition component.

The UHF-ECR etcher is capable of producing a medium density plasma over a large area at low pressure, thus ensuring a good vertical profile with minimum CD shift. In gate mask processing, step etch process is required to minimize the CD shift and ensure the selectivity of the underlying substrate, so in this case the magnetic field and antenna bias are used to regulate the rate distribution of each step so that the in-plane variation in the CD shift is held below 5 nm.

Since ArF resist has relatively weak resistance to plasma, the wafer temperature must be reduced, and the UHF-ECR etcher obtains vertical profiles through low-pressure processing even in the low-temperature domain. Fig. 6 shows processing examples for a 0.1µm gate mask.

## LOW-k FILM ETCHING PROCESS

A number of different material systems are now being evaluated for use as low-k interlayer dielectric material including SiOF, SiOC, and organic films. There is thus a ready demand for an etcher that can support etching processes tailored to these different materials. In dual damascene processing, a number of special issues must be addressed in order for the via hole and trench processing to be done consistently.

One of the virtues of the UHF-ECR etcher is that it is capable of producing stable gas pressures and plasma densities over a wide range, so it can be readily applied to low-k damascene process applications.

Next, we will briefly describe processing application examples for inorganic and organic films, respectively.

#### Inorganic Low-k Films

In interlayer dielectric processing using low-k film, via hole and trench processing are required. First, we consider the requirements for via hole processing: (1) Good vertical profile with no bowing



Wafer specifications: BARC/SiN/SiO2

Fig. 6—Examples of Gate Mask Etching. Excellent vertical profile and CD control are obtained by processing at low pressure, while excellent in-plane uniformity is obtained by controlling the magnetic field.

(2) Good selectivity with the mask material (PR: photo resist)

(3) Suppression of processing defects due to particles from the sidewall material

The requirements for trench processing are as follows:

(1) Good vertical profile

(2) Prevent abnormal shapes including fences and subtrenches

(3) Prevent chemical damage to the film

These requirements are largely the same as those mentioned earlier for the HARC process and gate mask etching.

Although the chemical conditions must be adjusted somewhat to accommodate the properties of different materials, essentially an optimum process can be constructed by applying the HARC process for the inorganic low-k film via hole process, and the gate process for the trench process, respectively.

#### Organic Low-k Films

For organic etching a good vertical profile mask selectivity is important, but in addition, it is also important that no residue is produced. Since damage to the film must be prevented and good profile control is required, hydrogen gas is generally used for the etching gas. This means that if sputtering strikes the chamber wall, material particles will be emitted into the plasma, thus resulting in residue and particles. Since high frequency is used in UHF-ECR etching, self bias (*Vdc*) at sidewalls is minor. For this reason, antenna bias control is used to minimize sputter while





By independently controlling the ion energy, excellent mask shoulder selectivity and non residue etching are obtained.

suppressing deposition on the antenna surface, so that there is relatively little residue and particles, and a stable process is achieved.

Little residue is produced by this process even when the wafer bias is reduced, so as a consequence the mask selectivity is increased (see Fig. 7). This process has already been applied to a commercial product, Hitachi's plasma process tool, and considerable experience has now been obtained with the process.

# CONCLUSIONS

This article provided an overview of the UHF-ECR dielectric film etching tool that was developed for the 90-nm technology node and beyond. Fabrication equipment for semiconductor devices must be capable of accommodating a wide range of process applications including high-aspect-ratio holes, masks, and low-k damascene processes. We are confident that by further enhancing the UHF-ECR system and improving the controllability of the plasma, Hitachi Group will be able to accommodate all of these needs.

#### REFERENCES

- S. Kadomura et al., "Low-k Films and Etching," Electronic Journal, 24th Technical Symposium, pp. 27-39 (1999) in Japanese.
- (2) T. Kawane, "Copper Damascene," *Semiconductor World*, pp. 82-85 (1998) in Japanese.
- (3) N. Itabashi et al., "UHF-Band ECR Plasma," *Journal of Plasma and Fusion Research*, Vol.73, No.12, pp. 1365-1373 (1997).
- (4) M. Izawa et al., "Study of High-selectivity Oxide Layer Etching by UHF-ECR Plasma," Preprints of the 46th Symposium of the Japan Society of Applied Physics, pp. 793-794 (1999) in Japanese.

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