Prospects for Si Semiconductor Devices and Manufacturing Technologies in Nanometer Era

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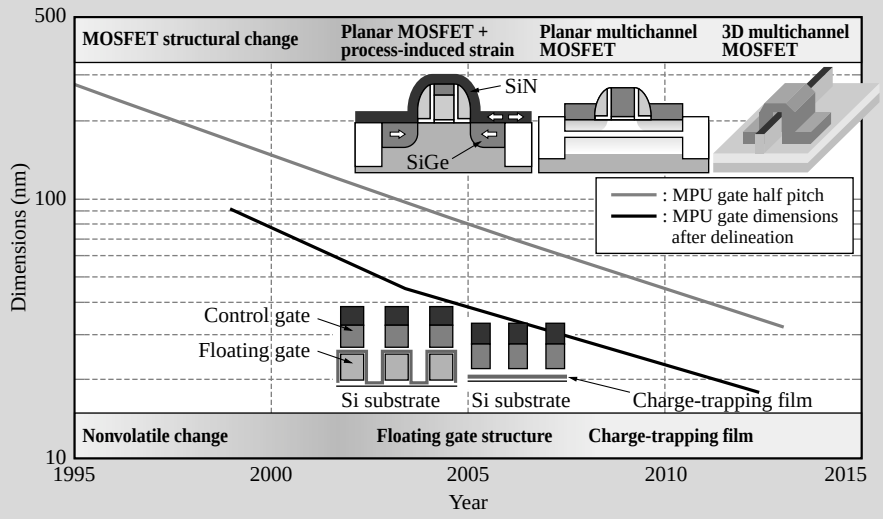
OVERVIEW: Now with the availability of devices based on 65-nm node microfabrication technology, the miniaturization of silicon LSI further progresses into the nanometer range. There have been many proposals as to how the conventional constraints of legacy Si devices might be superceded. Considerable interest has focused on a device structure in which current channels are fabricated on a 3D substrate for implementing basic Si-LSI MOSFET devices, and now Hitachi has developed a new type SOI-MOSFET that not only exhibits the same effects as 3D structure channel MOSFET devices but also takes full advantage of substrate bias. Enormous interest has also focused on nonvolatile memory for an expanding range of applications to new products—particularly flash memory, the mainstay high-density memory used today—but the memory cells for storing charge in conventional floating gates is limited. This led us to a new approach in developing a memory based on charge-trapping film. While pursuing this kind of ground-breaking work transforming individual silicon devices, Hitachi is committed to developing and providing the best LSI manufacturing technology solutions.

INTRODUCTION

WE published an article "Prospect of Si Semiconductor Device in Nanometer Era" two years ago in the July 2004 issue of "Hitachi Hyoron" (Vol. 86 No. 7)[(1)]. That article highlighted the basic MOSFET (metal-oxide semiconductor field-effect transistor) silicon device as especially promising as LSI technology continues to evolve toward smaller features. Now just two years later it is apparent that Si semiconductor devices and indeed the whole LSI sector environment have undergone profound changes. Against the backdrop of continued strong sales in digital home electronics and appliances, it is projected that the world semiconductor business including Japan will see



MOSFET: metal-oxide semiconductor field-effect transistor
MPU: micro processing unit

Fig. 1—Projected Structural Changes in Key LSI Devices: MOSFETs and Nonvolatile Memories.
Changes in MOSFET and nonvolatile memory device structures parallel progress in reducing the scale of micro fabrication capabilities. MOSFETs are expected to evolve by moving to 3D implementation of the channel region, while nonvolatile memories will advance by exploiting charge trapping films.

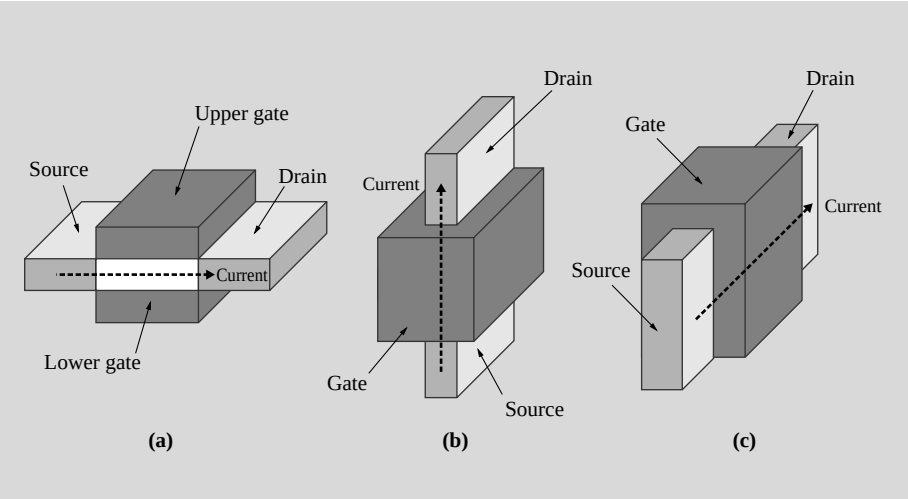


Fig. 2—Types of Multi-gate MOSFETs.
Three configurations: planar MOSFET (a), vertical transverse channel MOSFET (b), and vertical longitudinal channel MOSFET (fin-type MOSFET) (c).

renewed growth in the years ahead. But due to the pull-back in demand and lowering of prices that began around the end of 2004, many of Japanese device manufacturers experienced negative growth in 2005. Now it appears that dip is behind us, for we are seeing the emergence of new applications for high-density flash memory such as portable digital audio players that have become extremely popular within a short period of time. And manufacturers with a large share of the market for LSIs used in PCs and mobile phones have also seen a steady increase in sales.

On the technology front, some manufacturers have already started shipping logic LSIs based on 65-nm node micro fabrication technology. In the memory sector, we are beginning to see availability of flash memories based on 80-nm node technology.

Based on these changes over the past two years, we envision renewed prospects for silicon semiconductor devices and for LSIs in the coming years (see Fig. 1). This paper we will focus on 3D devices and nonvolatile memory—specifically, flash memory that has seen such dynamic recent growth—with emphasis on the performance and capabilities required by the fab and manufacturing technologies needed to keep up with ever-smaller device feature sizes.

3D MOSFETS

The ITRS (International Technology Roadmap for Semiconductors) projects that by the year 2010, a half pitch will be 45 nm and the gate length of high-performance MOSFETs will be 18 nm[(2)]. It would be exceedingly difficult to reach these dimensions with today's planar MOSFET structure.

As a way of breaking through the current constraints on further feature downsizing, multichannel MOSFETs with more than two gate electrodes have recently been attracting enormous interest. Multichannel MOSFETs control the MOSFET channel region with two or three gate electrodes, and thus are far more robust against short-channel effects and permit smaller features than conventional MOSFETs that control the channel region with a single gate. Multichannel MOSFETs can be broadly classified into the three structural types illustrated in Fig. 2:
(a) planar structure that is essentially the same as the conventional MOSFETs, and two non-planar or 3D configurations:
(b) a vertical transverse channel MOSFET, and
(c) a vertical longitudinal channel MOSFET.

Planar MOSFETs

Planar multichannel MOSFETs are essentially the same in structure as conventional MOSFETs, and therefore have the advantage of allowing continued use of the same legacy planar processing technology. The main drawback of the planar MOSFET is that self-aligned formation of the upper and lower gate electrodes is difficult and this complicates the fab processing.

Recently Hitachi and Renesas Technology Corp. found a way to significantly reduce these problems by developing a new and fairly simple technology for fabricating planar multichannel MOSFETs that avoids complex manufacturing processes [see Fig. 3 (a)]. The advantages of our new approach is that it thins the oxide layer buried in the SOI (silicon on insulator) substrate to 10 nm (versus 100 nm in conventional technology) and thus permits self-aligned upper and

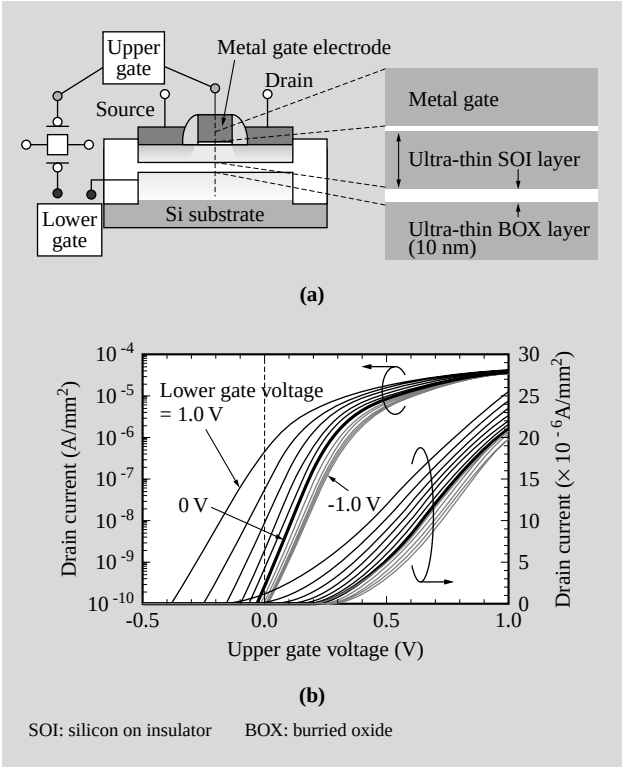


Fig. 3—Thin-film BOX-SOI Cross-sectional Diagram (a), and Switching Characteristics (b).
A key difference from the conventional SOI-MOSFET is that the BOX layer is thinned to approximately 10 nm. This permits modulation of the MOSFET characteristics by manipulating the substrate bias.

lower gate electrodes by forming the lower gate electrode using an impurity implantation technology[3]. In the conventional multichannel MOSFET, the gate electrodes were integrated and it was thus only capable of driving a three-terminal type device.

Using our new device structure called a thin-film BOX (buried oxide) SOI, the upper and lower gate electrodes can be controlled independently, thus permitting devices to be driven by four terminals. The bit advantage of the four terminal type is that it allows three gate electrodes to be used to freely control device threshold voltage while one of the gate electrodes is used to control device switching. Fig. 3 (b) shows the switching characteristics of a multichannel planar MOSFET that we actually tested. One can see from the figure that the device current changes very conspicuously by controlling the lower electrode bias. By exploiting this bias effect, output current is increased by 20% when the device is operating and the off leakage current is decreased when the device is in stand-by, so the performance is increased even though the device is consuming less power.

3D MOSFETs

The planar MOSFET device described in the July 2004 article in the Hitachi Hyoron corresponds to the vertical transverse channel MOSFET illustrated here in Fig. 2 (c)[1]. This was the prototype of the device structure that Hitachi later proposed[4]. This set the stage for a number of novel 3D MOSFETs including a double-gate MOSFET using two vertical channel walls as gate electrodes, an enclosed tri-gate MOSFET[5] using three channel cross-section surfaces as gate electrodes, a Pi gate structure MOSFET taking its name from the cross-sectional profile[6], and an omega (Ω) gate structure MOSFET[7]. All of these novel structures can be thought as falling into the category of fin structure MOSFETs, a device structure that effectively suppresses short channel effects using gate electrodes to improve the controllability of the channel region.

In another recent development, we are beginning to see a growing number of reports describing conscious efforts to increase integration. Some specific

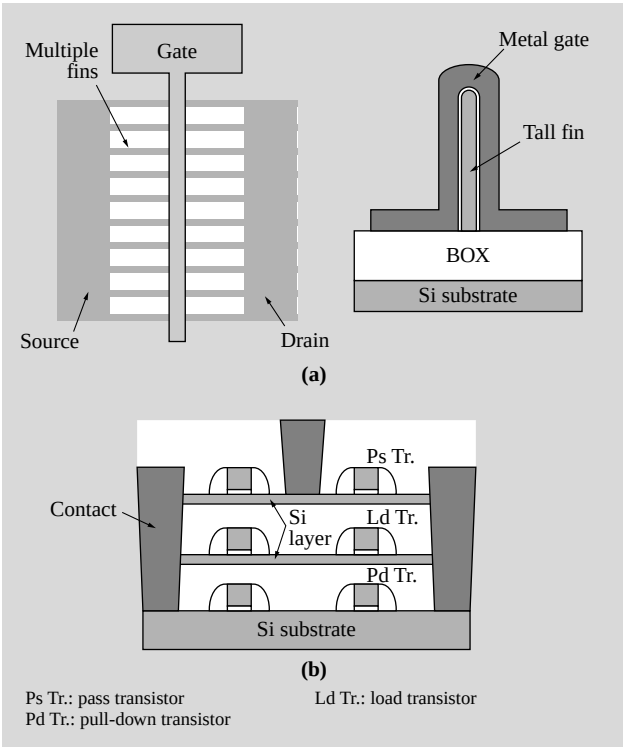


Fig. 4—Improved Fin Structure MOSFETs: MOSFETs with Multi-fin and Tall Fin Structures (a), 3D Structure SRAM (b). Typical MOSFETs featuring 3D channel structures. The designs have been implemented to increase current flow and permit stacking of devices.

examples include fin structure MOSFETs using metal gate material to modulate threshold voltage, and the multi-fin and tall fin MOSFET structure shown in Fig. 4 (a) that seek to increase the effective gate width area[8]. Because they employ such narrow fin profiles no more than several tens of nanometers wide, these structures effectively overcome the particular problem associated with fin MOSFETs of being unable to ensure sufficient gate width. A fin structure MOSFET-based SRAM (static random access memory) design has also been recently reported, and its circuit operation is currently being investigated[9]. While different from the fin structure MOSFETs we have been describing, the recent development of 3D structure SRAMs featuring 3D integration of planar MOSFETs[10] such as shown in Fig. 4 (b) underscores the recent movement toward 3D structure MOSFETs.

NONVOLATILE MEMORY

High-density Nonvolatile Memory

Along with the growing popularity of the portable digital audio players, the market for high-density nonvolatile memories (flash memories) as a storage medium has greatly expanded. Mainstream production today is based on 2-Gbit memories using 90-nm microfabrication technology, but 8-Gbit memories based on 60-nm technology have started to appear[11].

Fig. 5 (a) shows a schematic cross-section of the structure of a high-density flash memory memory cell, the smallest unit of memory. It consists of a polysilicon stacked structure with polysilicon blocks (floating gates) isolated by dielectric film (SiO_2) in the lower part. A 2-Gbit memory measures only about 80 nm × 100 nm × 100 nm. And as shown in Fig. 5 (b), control gates are formed above as electrodes. High voltage is applied to the control gates, and electrons are injected into the floating gates from the Si substrate to program the memory.

The biggest challenge facing the flash memory derives from the fact that the size of the floating gate and the spacing between gates only measures several tens of nanometer. As can be seen in Fig. 5 (a), the control gates must be buried in the gaps between the floating gates to ensure a sufficient coupling ratio. The essential difficulty was that the gap between floating gates is only about 50 nm and the ONO (oxide-nitride-oxide) layer that provides insulation between the control gate and floating gate had to be 15-nm thick, so there was no way that the control gates could be implemented in these microscopic gaps between floating gates any time soon.

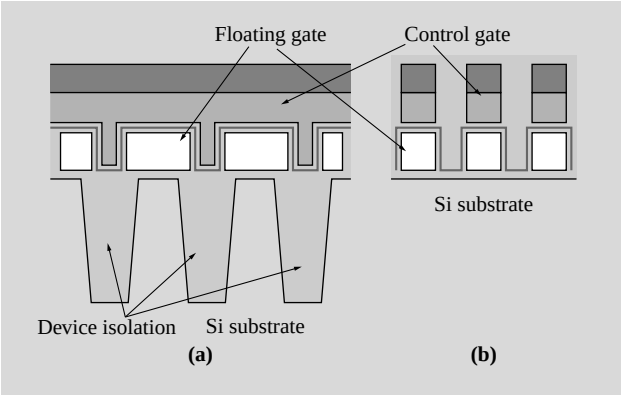


Fig. 5—Schematic Cross Sections of Floating Gate Type Flash Memory.
Lateral cross section of a control gate (a), and vertical cross section of a control gate (b).

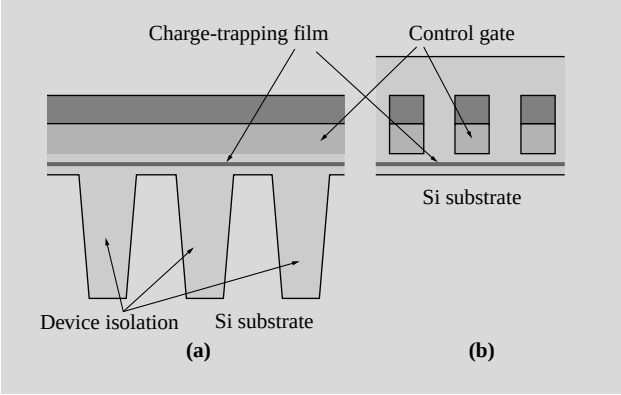


Fig. 6—Schematic Cross Sections of Flash Memory with Dielectric Film.
Lateral cross section of a control gate (a), and vertical cross section of a control gate (b).

This dilemma brought attention to the use of dielectric film instead of floating gates as the charge storage medium[12]. Fig. 6 shows a cross-sectional diagram of a memory adopting this approach. Silicon nitride film is used for its ability to store electrons and holes for a sufficiently long period of time. Specifically, the nitride film is sandwiched between two layers of oxide to form a multilayer ONO film structure. Voltage is applied to the control gate, electrons are injected from the substrate into the nitride film, and the electrons are captured at the interface between nitride and oxide films.

Hybrid Nonvolatile Memory

Future applications for nonvolatile memory is not just confined to high-density memories. For example, another application is the microprocessor in which flash memory is mounted on a microprocessor. The

basic role of the flash memory is to store the program that runs the microprocessor. Programs are read out of a special ROM (read-only memory), but the advantage of using nonvolatile memory is that the program can be easily updated and overwritten even when the final product is upgraded, thus reducing the product development cycle time and improving flexibility. Japanese LSI manufacturers are particularly well positioned in this area of flash microprocessors[13].

Although the nonvolatile memory used in flash microprocessors is essentially the floating gate type, it adopts a unique memory structure supporting fast writing, erasing, and reading of data. Fig. 7 shows a schematic example[14]. As one can see, the MOSFET is positioned so the control gate is immediately adjacent to the floating gate. For this reason, this type of MOSFET is referred to as a split gate structure. The control gate MOSFET opens the channel, and electrons flow through it. When this happens and high voltage is applied to the diffusion layer below the floating gate side, the electrons flowing through the channel speed up at the high electric field region near the boundary between the control gate and floating gate, thus achieving a high energy state and electrons are injected into the floating gate. Because the electrons are injected in such a high energy state, writing is done at a very low voltage. Erase operation is accomplished by applying positive voltage to the control gate that causes the electrons to be ejected. Use of the ONO film described earlier has already made its debut in flash microprocessors[15].

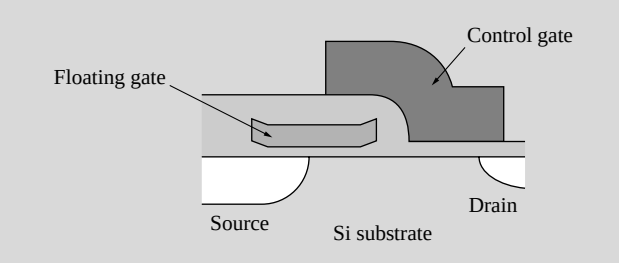
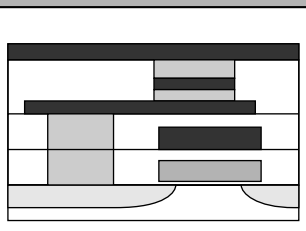
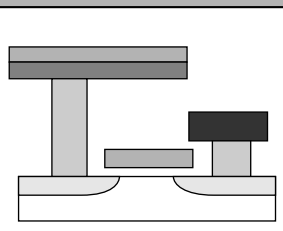
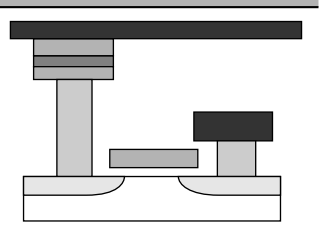


Fig. 7—Split-gate Structure of Nonvolatile Memory for Hybrid Use.
Floating gate and control gate are adjacent in this device called a split-gate-structure nonvolatile memory. Hot carriers from the control gate channel are injected into the floating gate.

Nonvolatile Memory Employing New Operating Mechanisms

Fig. 8 shows a comparison of some of the novel types of nonvolatile memory featuring new operating mechanisms. Here we will highlight three types: MRAM (magnetic random access memory), PCRAM (phase change random access memory), and RRAM (resistive random access memory). MRAM adopts the magnetic resistance effect exploiting the difference in magnetic moment orientation of magnetic materials sandwiching current flowing tunnel junction. The

Memory device	MRAM	PCRAM	RRAM
Device structure			
Data storage mechanism	Magneto-resistance change	Phase change	Resistance change
Material	FeMn/Co	GeSbTe	$Pr_{0.7}Ca_{0.3}MnO_3$, NiO
Cell size	8 – 15 F^2	8 – 15 F^2	4 – 6 F^2
Alignment with CMOS	2-3 additional masks	2 additional masks	2 additional masks
Voltage (current)	3 V (1 mA)	3 V (0.5 – 1 mA)	3 V (2 mA)
Overwrite cycles (number)	10^{15}	10^{12}	10^{6}

MRAM: magnetic random access memory
PCRAM: phase change random access memory
RRAM: resistive random access memory
F: feature size

Fig. 8—Comparison of Nonvolatile Memories Using New Materials.
Representative examples of new nonvolatile memories using new materials for the data storage part. MRAM exploits magnetic resistance change, PCRAM leverages resistance change between crystalline and amorphous phases, and RRAM utilizes resistance change occurring at the interface between metal and silicon.

magnetic substance consists of Fe, Mn, Co, and other materials, while the tunnel junction consists of an extremely thin Al_2O_3 film about 1-nm thick[16]. The PCRAM uses the difference in resistance resulting from changes in crystallographic phase (crystalline or amorphous) of chalcogenide (a ternary compound of germanium, antimony, and tellurium) film, a mechanism that has already found practical application in DVDs (digital versatile discs). PCRAMs use electric pulses to differentiate crystalline from amorphous material[17]. RRAM also exploits the resistance difference when current flows through metal contacting silicon[18].

Note that all of these new types of memory utilize resistance change. In order to cause this resistance change in storage media, it currently requires a current on the order of 1 mA per cell. All kinds of techniques have been tried in an effort to reduce the current[19], but still much more current is needed than in traditional memory devices. While there are still many obstacles, this kind of memory has a major advantage that simply cannot be achieved with legacy memory; namely, a superior write/erase capability of reportedly more than 10^{10} erase and write cycles.

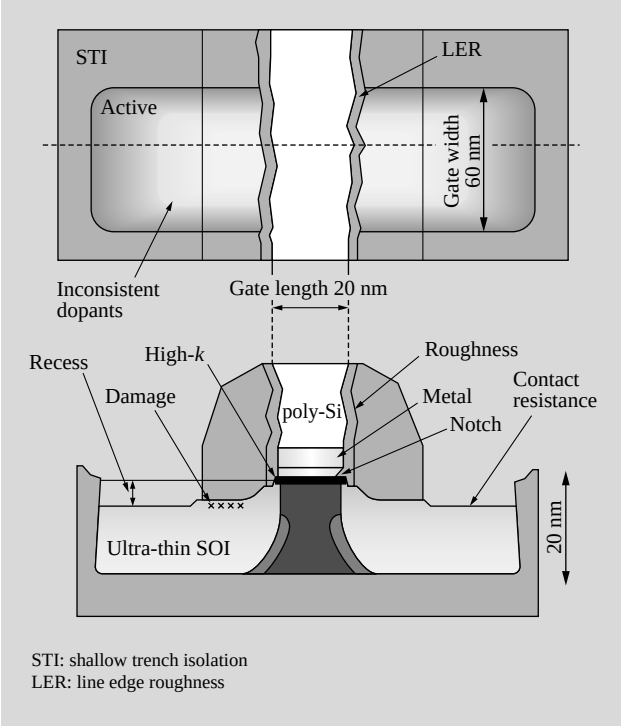


Fig. 9—Structure of Ultra-thin SOI Devices and Process Issues by Year 2010.
Future issues we assume will need to be addressed. As features sizes shrink and films become thinner, various problems are likely to emerge including roughness, substrate recess, and ion damage.

TECHNICAL ISSUES AND PROSPECTS FOR FUTURE DEVICE FABRICATION

Manufacturability as Device Geometries Continue to Shrink

We have emphasized that the minimum feature size of electronic devices is continuing to shrink, and we are also continuing to investigate new materials and new device structures. In this section we will first consider the challenges faced by manufacturing technology to accommodate shrinking device geometries. The ITRS[2] is assuming that ultra thin SOI MOS (metal oxide semiconductor) logic devices will evolve along the lines of the structure shown in Fig. 9. Both the gate length (L_g) and SOI layer are approximately 20-nm thick. The feature size tolerance is 2 nm at 3 σ. In atomic layers, this is only about 10 atomic layers, so in effect next-generation manufacturing processes require control capabilities at the atomic layer level. Fig. 9 highlights some of the new challenges that lie ahead: LER (line edge roughness), recess, and damage.

Tolerance for LER is on the order of 5 nm at 3 σ, and the component above a frequency of 100 nm is large[20]. As gate widths (L_w) shrink along with the exponential decrease in device dimensions, the variations in critical dimensions due to LER is a primary cause of gate length variation. This becomes especially apparent in the low power consuming devices for the 65-nm node and beyond. LER is generally attributed to resist materials and layout, and ongoing development is searching for ways to suppress LER[21]. Short-frequency LER is a relatively small component in the overall problem, but etching is being investigated as a way to improve this LER[22].

High-*k* materials are used in gate dielectric films, and the gate electrode is metal. Oxygen has a way of getting into interfaces between metal gate electrodes and polysilicon, and thus increasing the risk of defects. Undercut control known as "notch" is also critically important during processing[23]. It is likely that mid-gap metal will be used to control threshold voltage in ultra-thin SOI, but when using different materials for p-type and n-type, it is quite possible that damage will occur on the silicon substrate as a result of the different metals and different film thicknesses.

Damage to the silicon substrate can occur not only during the gate electrode processing but also during offset-spacer processing, and the potential for photoresist stripping is also problematic[24]. Up to now,

a damaged layer of several nanometers could be avoided by sacrificial oxidation or getting rid of it, but in channel formation in the years ahead there will not even be a tolerance of a several nanometers recess. Especially considering the proximity of the depth of the spacer oxidation film etching and the depth of boron ion implantation, it has been reported that damage caused during etching has effectively hindered connection[25]. Moreover, in the photoresist stripping after ion implant and etching, the nonvolatile material is implanted in the photoresist which requires high-power plasma processing, and as a result the amount of recess increases.

The impurity profile is extremely important because it determines the transistor characteristics, and here too a number of issues have emerged as feature sizes have continued to shrink. Especially where a steep profile is required, variation in depth due to polysilicon grain orientation and implantation exceeding the metal gate electrode are problematic. The ability to control the impurity concentration variation and profile control in the vicinity of STI (shallow trench isolation) is also becoming more important[26].

Regarding transistor characteristics, besides the patterned profile and impurity profile, the adverse effects of stress have been increasing. Channels with strained structures are effective for increasing speed, but considered from another perspective, stress causes threshold voltage to change. This has led to studies on ways to improve stable operation and increased speed of devices through stress control based on STI-induced stress and passivation layer formation[27]. For mass production, this will require assessment of stress control stability and quality control technology to perform the assessment.

Here we have highlighted some of the primary issues associated with ever-smaller feature sizes, but addressing these concerns will not only require more accurate critical dimensions, but also technological solutions to reduce LER, to suppress recess, and to effect better stress control. All of these challenges will require further development, including work on better metrology tools and better quality control methods.

Converting to 3D Devices: Manufacturing Challenges

Various 3D channel structures are being investigated for application to future transistors including multi-gate designs for logic and RCAT (recess-channel-array transistors) for memory[28]. Here we will consider some of these structural issues with reference to the FET structure shown in Fig. 10.

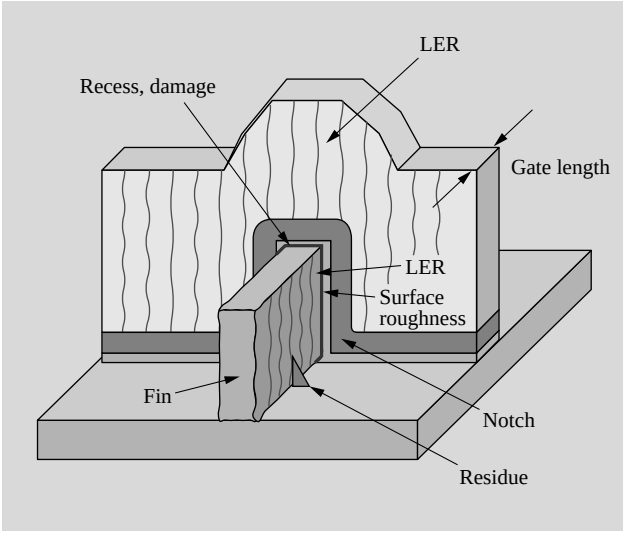


Fig. 10—Processing Issues Involving Fin Type FET Structure. Issues that must be addressed in fabricating fin structure FETs assuming existing process technologies. Process pattern profile control for structures with step height will become increasingly important.

From a manufacturing standpoint, the fin structure in Fig. 10 is more difficult than the planar structure in Fig. 9. In dealing with a fin structure FET, it is important to suppress surface roughness during processing in order to deposit a gate dielectric film. And in forming the gate electrode, critical dimensions and suppressing LER are just as important as with the planar structure, but the step height due to the fin increases the processing complexity. More specifically, over-etching is required that takes considerable time from the start of exposure at the top all the way down to the substrate. Time is required because the fin sidewall gate material must be removed. It has been reported that notching and residue related problems occur during over-etching due to this step-height issue[23), (29]. Processing is so much more exacting compared to planar structure devices that the prospects for damage to the upper part of the fin and recess will be major issues that must be solved.

Challenges and Prospects for Mass Production Technology

So far we have dealt with the manufacturing of individual devices. In this section we will review some of the technologies needed for the further advancement of mass production. The primary challenge of mass production is to supply the necessary volume during

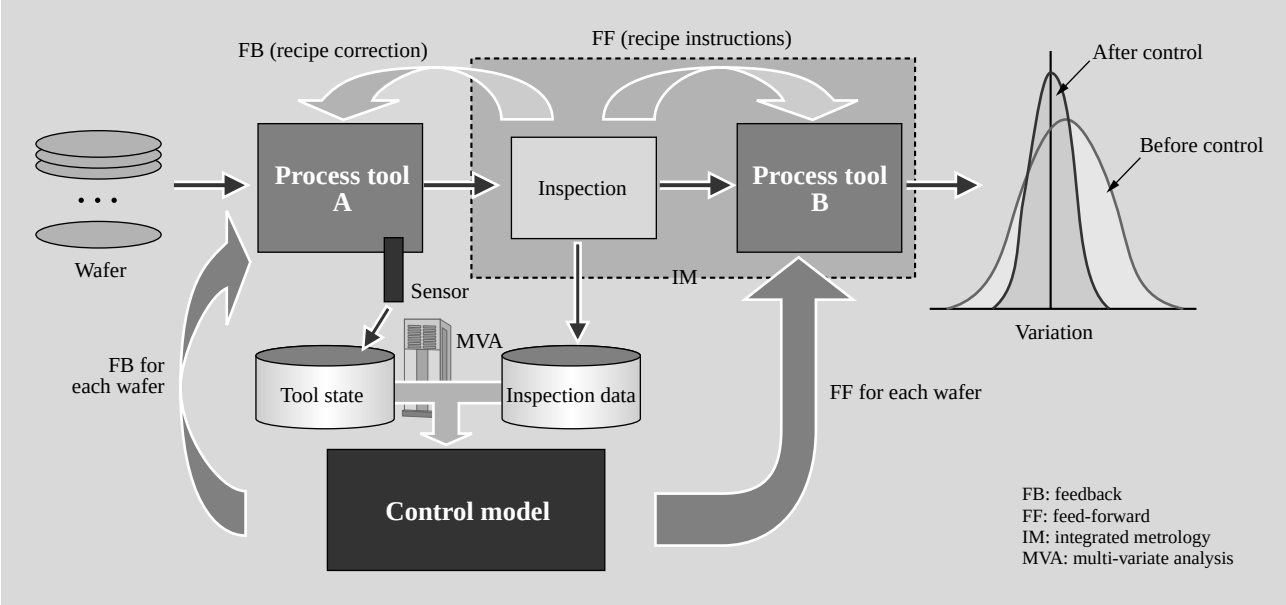


Fig. 11—Overview of Advanced Process Control Technology.
Process control based on wafer inspection data and tool state monitor data is essential for reducing variation in process pattern profiles.

the period when demand is high at costs corresponding to the market price. This means that cost, yield, and the interval until the product can be delivered are critically important. Meanwhile, as technology evolves toward ever smaller features, the costs of masks and lithography increase two-fold with each successive generation[30], so the importance of cost reduction also increases.

Fabrication processes that can accommodate smaller geometries have led to enormous efforts to develop tools that can achieve improved uniformity and repeatability. In order to improve the repeatability of processes, monitor feedback type process control is starting to be applied to etching and to CMP (chemical mechanical polishing). But as feature sizes shrink, tools being used at any given time reach limits as a result of differences between fabrication tools as well as the changes over time, so tool maintenance and other problems occur with greater frequency. This is dealt with by improving the comprehensiveness of tools, but this takes time and drives up costs.

Recently this has led to very vigorous efforts to put in place APC (advanced process control) systems such as illustrated in Fig. 11 to minimize variations between tools using FB (feedback) and FF (feed-forward) process controls. FF- and FB-based controls using wafer inspection data have emerged as the mainstream approach, and have now been widely adopted for stabilizing variations between lots.

Use of inspection data is generally restricted to the control of lot units, due to time responsiveness. This means that major changes can be corrected, but more precise process control in line with smaller features is not sufficient. For this reason, emphasis has shifted away from lot-to-lot control toward wafer-to-wafer control technologies[31].

But control on a per-wafer basis involves an enormous increase in the number of inspection steps, which sacrifices cost and throughput. Thus, high-speed inspection tools are mandatory. OCD (optical critical dimension) measurement requires a particular kind of inspection pattern, but it does support fast throughput and critical dimension measurement. More recently, new manufacturing tools using IM (integrated metrology) have been incorporated in the wafer transport area, and systems are now becoming available that significantly improve inspection efficiency.

On the other hand, these technologies still have not been incorporated in all inspection and measurement tools, so realtime control based on tool monitoring has been proposed[32]. By successively sensing the operating state of tools and performing multi-variation analysis on inspection data, a control model is constructed. In this approach, processes are predicted and tools are controlled from sensing data based on

the model. For example, it has been demonstrated that gate dimensions can be directly predicted from optical emission spectrum during the etching process[33].

This kind of sensing technology is being adopted because it has other advantages from a manufacturing standpoint. For quality control purposes in mass production, tool QC (quality control) and process QC are periodically conducted. The problem is that the tolerated range for each QC check becomes very rigorous, so that even a very minor tool change that occurs between QC checks is not overlooked. And thinking in terms of efficiency, increasing the frequency of QC checks is not desirable. One proposed solution is to not just implement 100% inspection as a single FDC (fault detection and classification) method, but rather a QC method using the control model described above based on tool sensing data[34].

DFM (design for manufacturability) is commonly invoked, but there is no question that design rule development procedures that take fab line yields into account and mask pattern optimization technologies are critically important. PPC (process proximity correction) as a mask feedback technology including exposure and etching steps has also been proposed[35]. CAA (critical area analysis) has also been implemented as a method for optimizing design rules in line with fab line yield performance[36].

DFM is also important, but considering that the gains from reducing differences between tools are now approaching the point of diminishing returns, greater emphasis will shift to process stabilization through realtime tool calibration.

CONCLUSIONS

In this paper we surveyed the current state and prospects for silicon devices as we enter the 65-nm node era, and also described some of the key manufacturing technologies needed to fabricate these devices. We described how devices and fabrication technologies are evolving to meet the challenges of ever smaller device dimensions. It is starting to become apparent that we can expect fewer integration and performance gains by relying solely on device miniaturization, and this is reinforced by recent developments: the use of process strain and 3D structures to boost the performance of devices, and the use of new materials in developing novel kinds of nonvolatile memory. In manufacturing technologies, the ability to suppress variation in devices plays a critically important role, and control tolerances on the order of several nanometers are now required. Clearly, technologies for integrating processes, devices, circuit design, and manufacturing will become increasingly important as time goes on. While remaining in the forefront of these developments, Hitachi is committed to provide the best solutions for manufacturing the highest quality and most efficient advanced semiconductor devices.

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