Current Status and Outlook of 3D Inspection Analysis for Semiconductor Devices

—Efforts Towards Smart Route-cause Analysis by New Measurement and Analysis Technology—

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OVERVIEW: In recent years, as the structures of semiconductor devices have been successively scaled down in an extreme manner, such devices have become more multi-layered and 3D. Consequently, as conventional measurement methods are becoming impossible to use, the difficulty of simple interpretation is becoming a major problem in defect inspection. As regards wafer-surface unevenness, cross-sectional shape of 3D structures, and breakage and short-circuiting of internal structures—which are all included in this problem—Hitachi High-Technologies Corporation provides solutions through its line-up of measurement, inspection, and analysis equipment. Utilizing specific examples, this report describes the present status of 3D measurement and inspection as well as 3D analysis, and describes the outlook for these technologies.

INTRODUCTION

AS regards improvement in development time, production yield, and reliability of semiconductor integrated circuits (LSIs), it is necessary to utilize metrology, inspection and analysis tools in compliance with these goals. Accordingly, as described in detail in the followings, Hitachi Group is providing metrology, inspection, and analysis systems aimed at the evaluation of cutting-edge LSIs. Moreover, in response to the year-by-year increases in the complexity of LSI structures, Hitachi High-Technologies Corporation is putting forward and

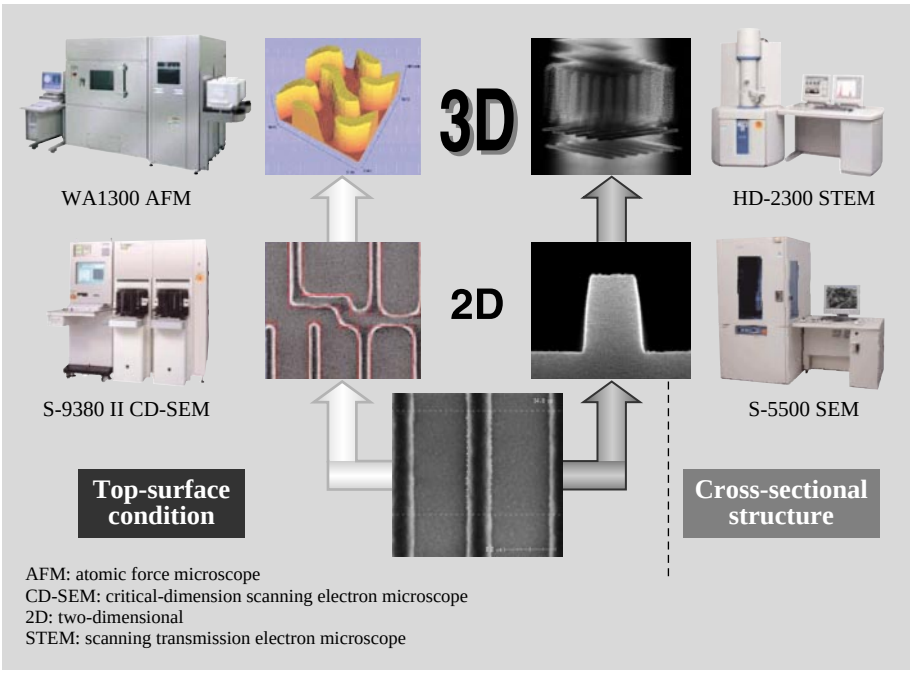

Fig. 1—Hitachi High-Technologies' Measurement, Inspection, and Analysis System Realizing Smart Root-cause Analysis.
A measurement, inspection, and analysis system of Hitachi High-Technologies consisting of four main components: CD-SEM for in-line measurement of pattern dimensions of semiconductor fine structures; AFM for high-precision measurement of flat surfaces up to 3D shapes; a linked FIB (focused-ion-beam) processing device for pinpointing and cutting out measurement image patterns on a 3D analysis holder that enables high-magnification observation and measurement; and an STEM.

energetically developing a method called "smart root-cause analysis" for advancing cause investigation of defects as the ultimate goal of evaluation analysis (see Fig. 1). Implementing smart root-cause analysis is anticipated to improve not only the efficiency of analysis, but also that of defect investigation and countermeasures.

In the present report, as one of the 3D inspection-analysis technologies being developed by Hitachi Group, smart root-cause analysis is first briefly overviewed, and its future prospects are outlined.

NEED FOR 3D INSPECTION AND ANALYSIS OF SEMICONDUCTOR DEVICES

The structure of a typical 3D device (a Fin-FET: field effect transistor) is shown in Fig. 2. A channel (i.e. "fin") through which current flows as a result of single-crystal silicon formed on SiO_2 is formed. A gate electrode is then formed in a manner straddling this fin. With excellent characteristics, such as suppression of the short-channel effect accompanying the scaling-down of devices, this device structure can replace the conventional planar structure from the 32-nm technology node and beyond[1].

As for the dimensions of the gate electrode, which are critical parameters that determine transistor performance, they are measured with high precision by methods such as CD-SEM (critical-dimension scanning electron microscope). With the scaling-down of devices—even in the case of the conventional planar structure—the need for measurement of side-wall angle as well as gate-electrode dimensions is getting stronger. In the case of a Fin-FET, which has a 3D structure, to control transistor performance, it is necessary to measure and control more feature sizes and dimensions. Even for a single gate-electrode dimension, it is said that a measurement value for each section along the channel is needed. Moreover, as dimensions of the channel itself, width, height, and corner radius must also be measured. Actual minute dimensions, that is, channel width of 10 nm and height of 60 nm at a gate-electrode width of less than 40 nm, have been reported[2].

A cross-sectional TEM (transmission electron microscope) image of a multilevel interconnection configuration device is shown in Fig. 2. However, note that in the case of microprocessors, similar examples of configurations with 7, 10, 11, and even 12 layers have been reported. As regards such multilevel interconnection configurations, even if failures are identified by electric tests, it is extremely difficult to determine whether defects exist in certain places. Accordingly, a pinpoint analysis technique based on failure location data is becoming ever more necessary.

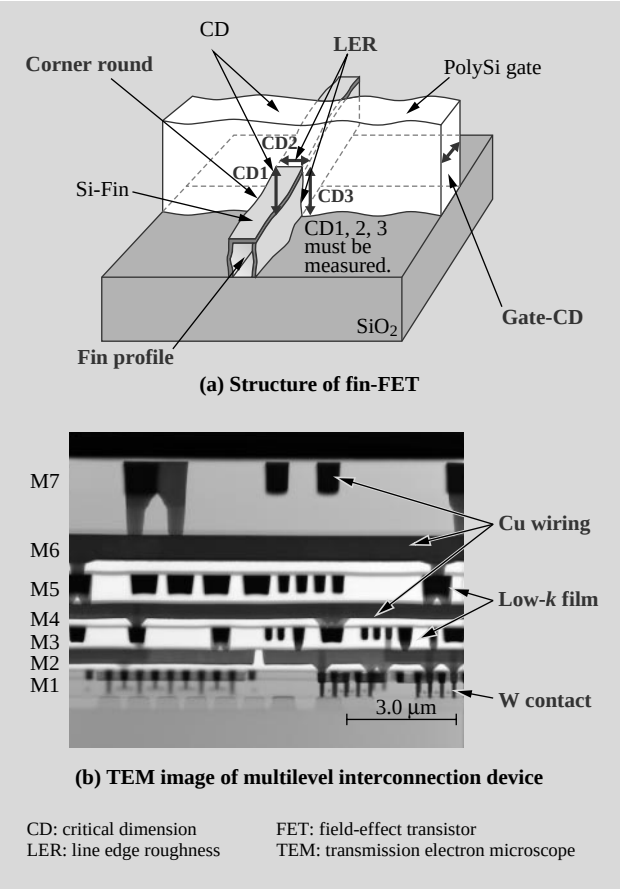

Fig. 2—3D Inspection and Analysis of Semiconductor Devices. (a) Structure of Fin-FET (typical 3D device) and (b) TEM image of multilevel interconnection device are shown.

CURRENT STATUS OF 3D INSPECTION AND ANALYSIS TECHNOLOGY

Simple Multi-dimensional Measurement Evaluation

(1) Measurement

In the field of CD-SEM, technical developments—such as the shift from conventional 1D-representation dimension measurement to 2D feature-size measurement, roughness measurement, 3D feature-size process monitoring—are pushing ahead. The details on our latest device and new measurement systems are reported in another paper[3].

(2) Irregularity determination of surface defects

The LS series of wafer-surface inspection systems, the IS series of dark-field wafer inspection systems, and the RS-4000 classification SEM for reviewing the defects detected by these two systems are fitted with a

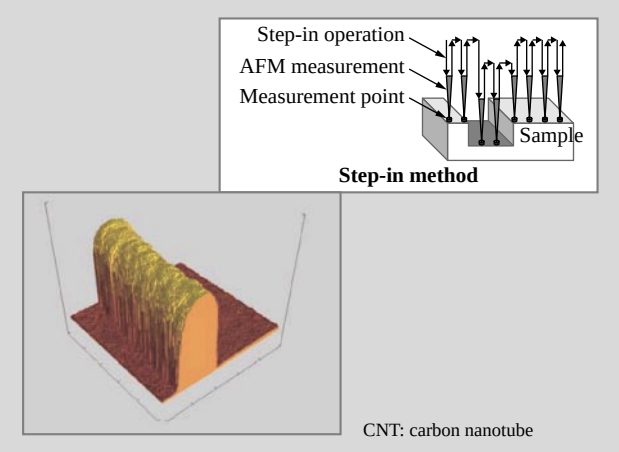

Fig. 3—Example of Analysis of Resist Pattern by AFM. A CNT probe is fitted in a wide-area AFM, and measurement is performed by the step-in method (which provides good shape traceability).

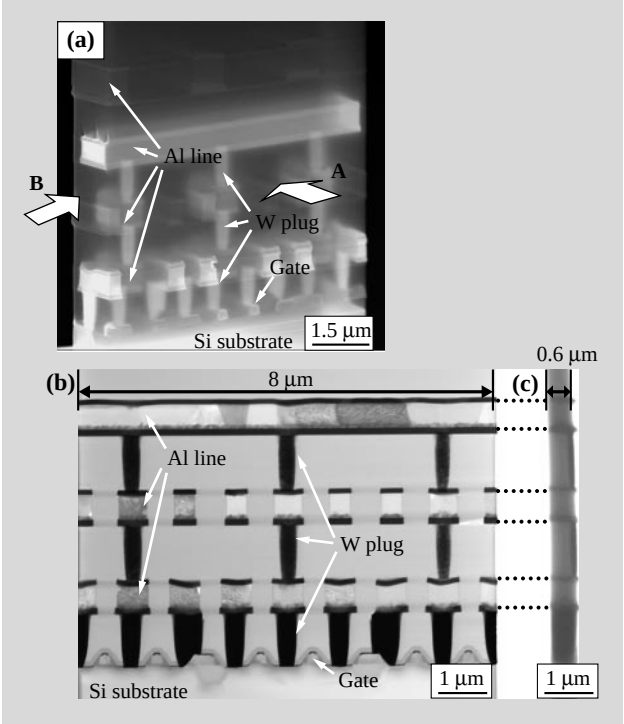

Fig. 4—3D Analysis of SRAM by Scanning TEM. Secondary-electron image: sample size: 2 × 8 × 10 µm (a), bright-field scanned transmission image taken from A direction (b), and bright-field scanned transmission image taken from B direction: sample size: 0.6 × 8 × 10 µm (c).

function for concavo-convex judgment on the detected defects.

Though this concavo-convex judgment for determining whether defects on the wafer top surface are bulges or depressions is performed in simple 3D inspection, it provides valuable information for root-cause analysis of defects.

3D Analysis

(1) 3D analysis of external structure (AFM)

AFM (atomic-force microscopy) is a way of realizing the finest 3D measurement analysis of a surface structure. AFM utilizes atomic force to measure sample surface features with nanometer-order depths and form traces of these features, thereby enabling measurement of 3D forms. Along with the increased importance of 3D information for LSI process management, non-destructive measurements of LSI steps, flatness, and roughness in the clean room are becoming necessary. Satisfying the above-stated needs, the WA series of AFMs of Hitachi Kenki FineTech Co., Ltd. is being operated at several LSI manufacturers.

Hitachi is also making vigorous efforts to develop the AFM probes accompanying these devices.

A CNT (carbon nanotube) probe manufactured by Hitachi Kyowa Engineering Co., Ltd.—utilizing technologies of Hitachi's Materials Research Laboratory—achieves high reliability and long lifetime, good compatibility with high-precision step-in method, and stable, high-precision measurement. Fig. 3 shows an example of measurement of a resist pattern by CNT probe, and captures the top feature shape well.

(2) 3D analysis of internal structure (3D-STEM)

To analyze the internal structure of a fine LSI, STEM (scanning TEM) is used. STEM scans an electron beam with a diameter less than 1 nm on to the surface of a thin-film sample. To observe the transmission image thus produced, and the images generally obtained are projected in 2D. With this method, overlapping information on actual 3D structures cannot be obtained. Accordingly, the sample is formed into a columnar structure without layers, and observing the sample from multiple angles makes it possible to directly observe 3D structures. This method uses micro-sampling with a focused ion beam and a 3D analysis holder for common use with FIB (focused ion beam)-STEM with a 360° rotational sample stage.

By focusing the ion beam on the analysis spot inside a wafer and chip, the micro-sampling method can cut out sample sizes suitable for observation from different shapes and fix them to the sample stage. An example observation of such a cut-out SRAM (static random-

access memory) is shown in Fig. 4. A 2D electron image of a device extracted from a rectangular solid (with length of 2 μm, width of 8 μm, and height of 10 μm) viewed diagonally from above is shown in Fig. 4 (a). By using a beam accelerating voltage of 200 kV, it is possible to clearly observe not only the sample surface but also the internal structure on the backside of the surface. Moreover, the thickness was further reduced to 0.6 μm by the FIB, and bright-field STEM images were taken from directions A and B indicated by arrows in (a) and shown respectively in Fig. 4 (b) and (c). By means of STEM, it is possible to observe internal structures even at thickness of 8 μm, and in the case that observation from direction A only is difficult, the difference in the positions of the tungsten plugs of the upper-side second step and the third step can be observed from direction B.

EXAMPLE OF 3D ANALYSIS AND THE EFFECT OF 3D CONVERSION

From now onwards, in addition to being further scaled down, device structures will continue to become 3D; 3D evaluation techniques will thus become indispensable. For example, in the case of device sizes in the range of several tens of nanometers, at the sample thickness used in general TEM, i.e. 100 nm, multiple device structures are present, and 2D projection images are no longer effective for correct analysis of 3D structures. A pattern diagram of a Fin-FET with a 3D structure is shown in Fig. 5 (a), and bright-field STEM images of the structure are shown in Fig. 5 (b) and (c). As already mentioned, in a Fin-FET, to control transistor performance, it is necessary to measure a great number of parameters. In this example, however, an evaluation example of the cross-sectional shape of a channel at the end of the gate electrode is shown.

First, an FIB was used to encompass the spots to be observed, and a columnar sample with 200-nm angle was formed. After that, STEM images were taken from two orthogonal directions. In doing so, the region in which the channel cross section is observed is confirmed, superfluous regions are eliminated by the FIB, sample size is trimmed to 100 × 200 nm, and bright-field STEM observation was performed from two directions [see Fig. 5 (a) and (b)]. In the STEM image taken from direction A [image (b)], gate shape and size can be assessed. From this direction, however, as regards the channel region, only the height can be assessed. On the other hand, by observation from direction B, it is possible to assess cross-sectional shape and size of the channel. For evaluation of future devices with 3D structures in the way described above, Hitachi considers that methods for multi-direction observation by STEM will become more and more important.

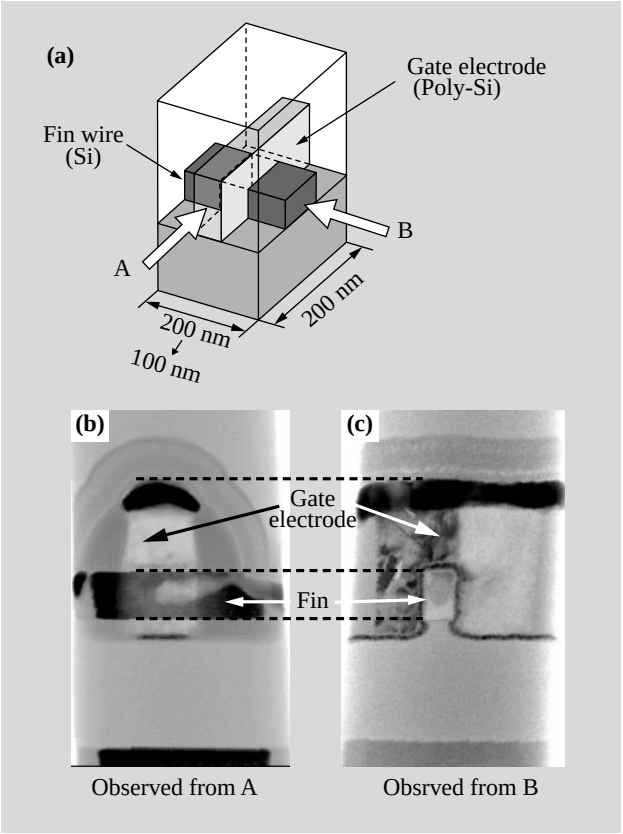

Fig. 5—Structure of Fin-FET.
(a) Pattern diagram of a Fin-FET with 3D structure,
(b) bright-field STEM image taken from direction A, and
(c) bright-field STEM image taken from direction B.
Final sample size: 100 × 200 nm.

CONCLUSIONS

Hardware technology for 3D inspection and analysis of LSI devices is making striking progress. As reported, the information volume obtained from 3D investigation and analysis is growing exponentially.

From now onwards, information-processing technology for adequately refining this increased information volume to enable investigation of targeted defects and setting up of necessary countermeasures will be further upgraded. Accordingly, Hitachi High-Technologies is providing “smart root-cause analysis” for simple and prompt handling of defect counter-measures for scaled-down, multi-layer LSIs.

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