New World of CD-SEM in Utilization of Design Data

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OVERVIEW: The widespread adoption of immersion lithography[(1)] has accelerated the trend toward ever-smaller semiconductor device features. Yet lithography is still fraught with difficulty, and the frequent use of super-high-resolution technologies is indispensable to ensure process tolerances. At the same time, the complexity of optical proximity correction to compensate for pattern distortions (the proximity effect) and the growing adverse effects of mask errors are still major challenges. It would be exceedingly difficult under these circumstances to efficiently raise device yields based solely on the conventional measures dealing with defects caused by particles, and new capabilities permitting measurement of hot spots that are vulnerable to defects is very much desired. Also required is better implementation of design for manufacturability that traces back to the design stage to preempt potential problems before they occur. With the idea of implementing such an approach, we developed DesignGauge, a system that automatically generates metrology design recipes based on design information. This tool not only fully automates the generation of design recipes, it also quickly and efficiently measures systematic defects that can be attributed to pattern design or tool characteristics. We improved measurement accuracy through statistical data sampling and developed measurement techniques for application to the most advanced 3D structures. This has contributed significantly to the quality and manufacturing efficiency of next-generation node devices by incorporating these capabilities in Hitachi's state-of-the-art metrology SEM systems.

INTRODUCTION

The CD-SEM (critical dimension scanning electron microscope) is a primary tool and used extensively in semiconductor processes, most often for performing simple one-directional measurements. But as features sizes on ICs (integrated circuits) have continued to shrink, the number of measurement points has multiplied and this has caused measurement efficiency to deteriorate to accommodate longer times needed for actual measurement and for setup. And coping with a decline in measurement reliability due to resist pattern roughness and damage from the electron beam used in the process has also become an enormous issue. Meanwhile, new requirements for automated

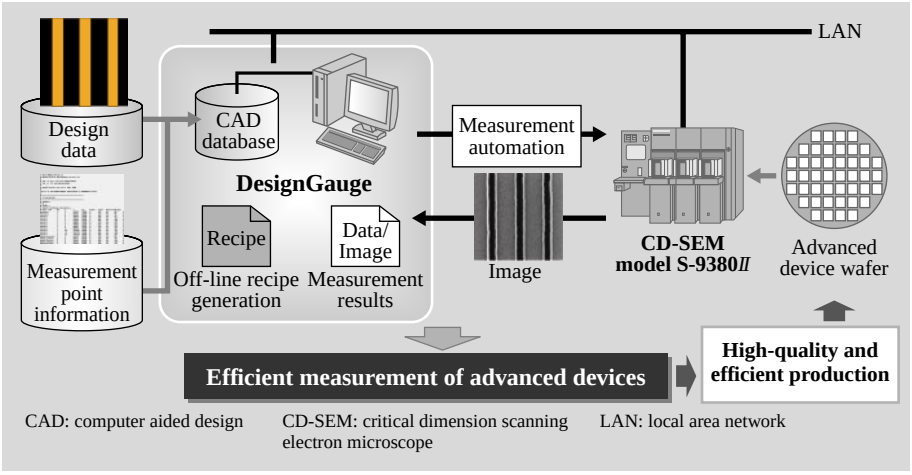

Fig. 1—Metrology SEM System Based on Design Information. The design information-based metrology SEM system is indispensable: by extracting automatically generated metrology recipes and pattern variations from SEM images, then verifying and comparing SEM images against simulation results, the system efficiently inspects the degree of transferred image deformation and identifies defects and hot spots.

metrology recipe generation for DFM (design for manufacturability) and the ability to measure hotspots based on systematic defect location information is becoming increasingly important.

Turning to lithography technology, the availability of immersion lithography has opened the way to high NA (numerical aperture) lenses. It is generally assumed that this will at least support development through the 35-nm technology node. Measurement technology has also seen progress in applications addressing reduced depth of focus and improved measurement accuracy. Based on the key idea of utilizing design information, this paper surveys the latest advances in measurement technology to support emerging measurement requirements of advanced IC processes (see Fig. 1).

CHALLENGES FACING NEXT-GENERATION LITHOGRAPHY MEASUREMENT TECHNOLOGIES

Systematic Defects in Lithography

An arsenal of measures are needed to reduce defects and boost yields of lithography processes. Fig. 2 shows an overview of the principle types of defects that occur. Most basically, defects can be grouped into two categories based on their cause: random defects caused by particles in the photoresist layer or introduced by process tools, and systematic defects that relate to the pattern design or the characteristics of the aligner or other tools and tend to occur in predictable locations. Since systematic defects tend to occur in specific predictable sites depending on their cause, they are endowed with coordinate information. Systematic defects can thus be effectively dealt with by accurately identifying the cause and adopting appropriate countermeasures. Among potential causes, OPC (optical proximity correction) errors and lens aberration will be major sources of defects in now emerging and next-generation lithography, so measures for detecting and dealing with these specific kinds of defects are urgently needed.

3D Measurement Technology

The shape of resist patterns is affected by a variety of factors—projected optical image, the resist material, the development process, etc.—and a great variety of patterns can be deposited. Fig. 3 illustrates the main factors for a typical pattern.

The pattern will later be amended by etching, and the feature patterns of the processed layer exhibit variation. Vertical processing of patterns is particularly desirable as pattern features continue to shrink, and it

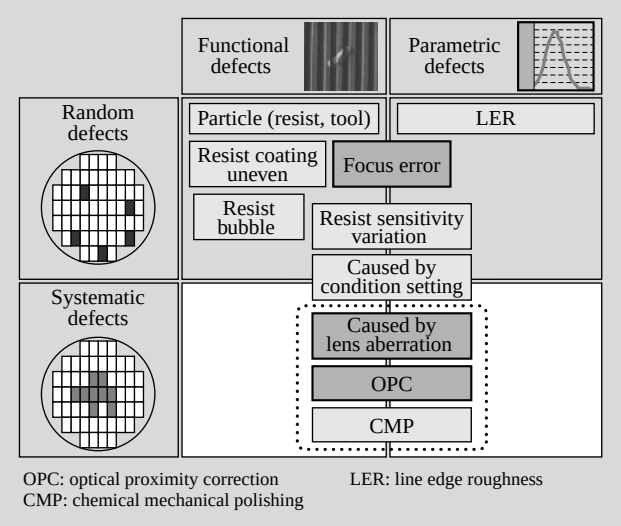

Fig. 2—Types of Lithography Defects. Categorized as random defects or systematic defects.

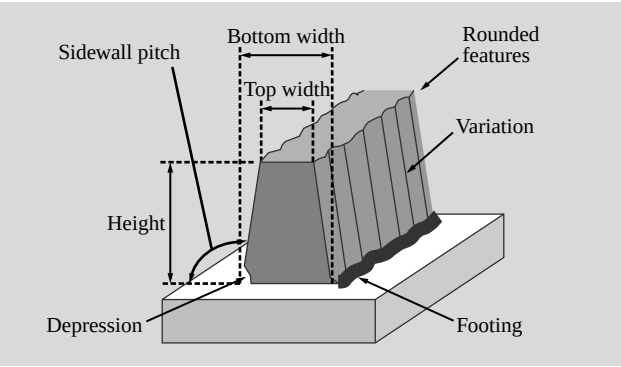

Fig. 3—Resist Pattern Design Requirements. Assessment points of resist sidewall pitch information, top width, bottom width, and footing.

is necessary to evaluate pitch information of the resist pattern sidewalls, the top width, the bottom width, and the residual resist at the interface with the substrate (the footing).

In pattern formation using a next-generation high-NA lens, the reduced depth of focus will also affect pattern formation, as illustrated in Fig. 4. Particularly at the ends of patterns, the angle of pitch of resist sidewalls changes significantly in the out-of-focus direction, even to the extent that reverse taper sometimes occurs. Measurement errors due to lens aberrations and OPC calibration errors also occur, thus making local measurements mandatory.

CD-SEM MODEL S-9380*II* FOR 45-NM NODE DEVICES

CD measurement at the 45-nm node demands better resolution and metrology repeatability, but also must

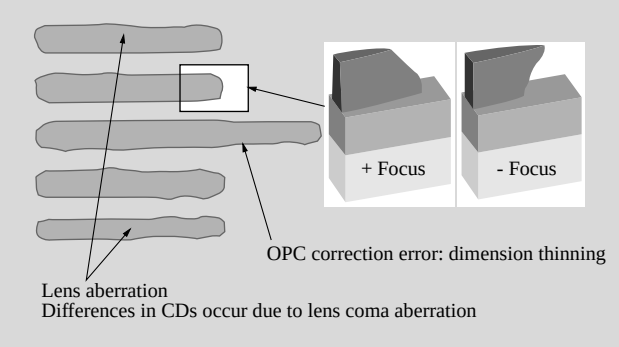

Fig. 4—Need for Local Measurement of Resist Patterns. Differences in CD occur around outer edge of pattern groups due to lens coma aberration. Pattern changes are most marked at the ends of patterns, resulting in reverse taper.

Fig. 5—CD-SEM Model S-9380II for 45-nm Node Processes. Capable of dealing with pattern roughness that becomes more pronounced as feature dimensions shrink and new 3D pattern designs.

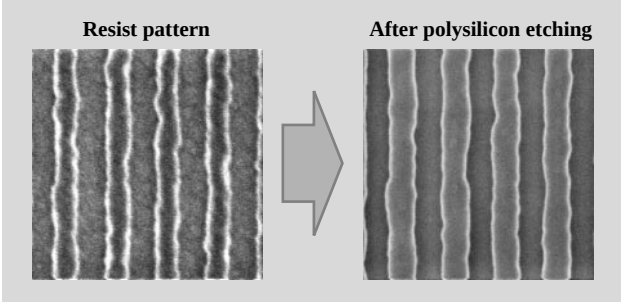

Fig. 6—Examples of Dimensional Variations of Resist Patterns in Length Direction.
These resist pattern variations were observed in an actual sample after dry etching.

be capable of dealing with the new challenges of significantly greater pattern roughness as feature sizes shrink and measurement of 3D structures. Hitachi High-Technologies developed a model S-9380*II* shown in Fig. 5, the company's most advanced CD-measurement SEM for the 45nm process node. In this section we will consider the exceptional performance of Hitachi's CD-SEM model S-9380*II*, and highlight some aspects of CD-SEM measurement technology for the 45-nm node.

Efforts to Enhance Basic Performance

Technical development relating the semiconductor processing is guided by the recommendations of the International Technology Roadmap for Semiconductors (ITRS). Required specifications have been defined for measurement technologies and for CD measurements alike, and development in this area if focused on meeting these requirements.

Today Hitachi High-Technologies has the largest market share in this sector (according to Data Quest 2004), and Hitachi's most advanced CD-measurement SEM is the model S-9380*II*, a system that offers superior measurement precision, resolution of 2.0 nm at an accelerating voltage of 800 V, and metrology repeatability of 0.6 nm at 3 σ. As one of the foremost manufacturer of electron microscopes, Hitachi High-Technologies already had a good headstart with the electron optics core competence to develop an electron-optical column with the world's highest resolution. By improving the performance while reducing aberration of its lenses, Hitachi's commitment to even better resolution and metrology repeatability remains unchanged, but Hitachi is also developing new materials to go along with more diversified devices, measurement technologies addressing new processes, and application technologies to meet users' needs. Here we will highlight some of Hitachi's recent measurement technology contributions.

Dealing with Pattern Roughness

Over the last few years, problems of line pattern LER (line edge roughness: variation in the length direction) and LWR (line width roughness: variation in line width) have emerged as major challenges (see Fig. 6). Gate pattern roughness in particular can have an enormous influence on the characteristics of transistors, and this is why detailed analysis of roughness is so important. LER is manifested as variations in frequency with both high and low frequencies present, and the precise measurement of these values is important because they are required for the analysis of transistor characteristics. Yet LER also causes reduced measurement repeatability, so there is strong demand for measurement that eliminates

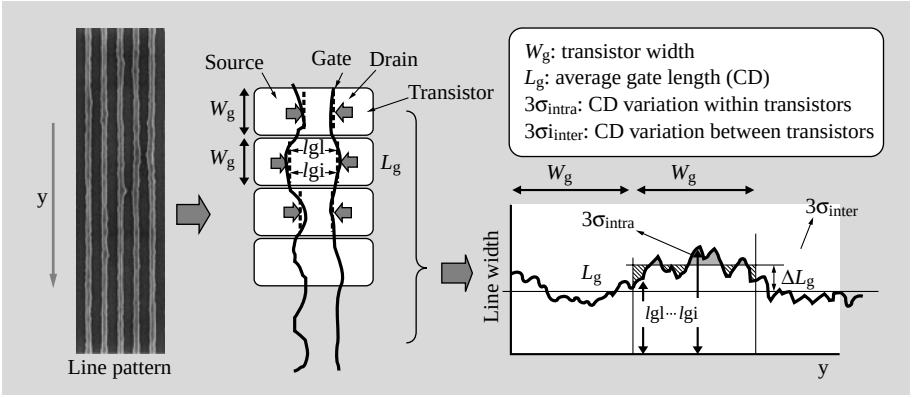

Fig. 7—Evaluation of LER and LWR (line width roughness). Image patterns are divided into numerous short segments in the length direction for CD measurement. This permits distribution analysis of CD variation in the length direction, and measurement of CD variation within transistors, CD variation between transistors, and average dimension measurements.

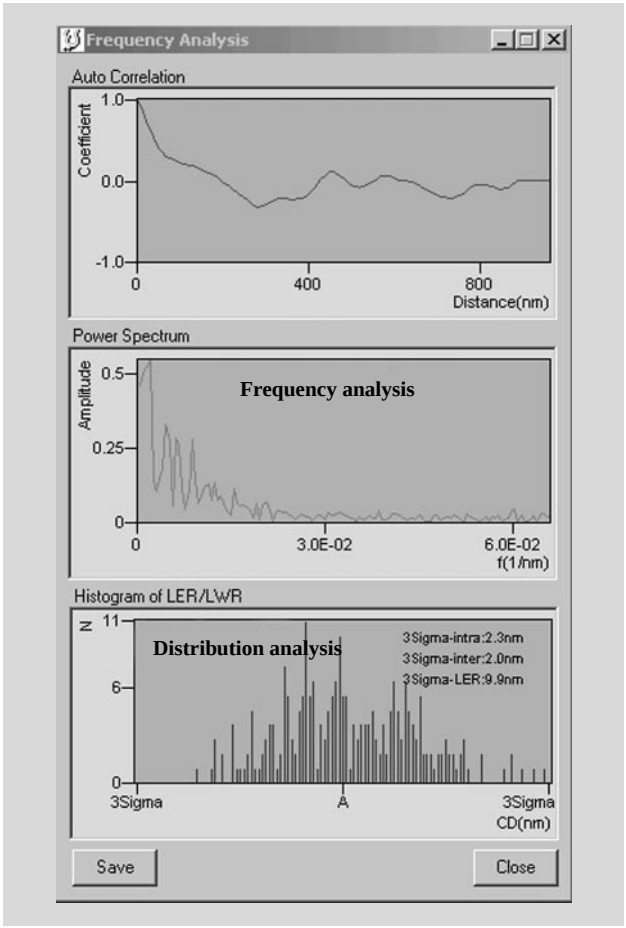

Fig. 8—LER Analysis Function.
CD variation distribution analysis, frequency analysis, and other types of analysis are supported (PC functions for data analysis).

the effects of LER. Actual LWR in recent ArF (argon fluoride) resists is on the order of 3–6 nm, roughly an order of magnitude greater typical CD measurement repeatability, and this is a source of erroneousness in measurements used for monitoring process stability.

In LSI processes for the 45-nm node and beyond, the relative proportion of LER to target dimensions will be even greater, thus clearly necessitating technologies that can reduce LER and also measurement algorithms that can accurately represent the measurements. In response to these needs, Hitachi's CD-SEM model S-9380*II* comes equipped with LER measurement capability (see Figs. 7 and 8). Essentially, LER is measured by dividing up pattern of interest into many short segments in the length direction, which are then CD measured. Then, through statistical analysis, the system supports CD variation distribution analysis in the length direction, frequency analysis, and average dimension measurements. The CD-SEM model S-9380*II* is also equipped with an ACD (averaged CD) function that helps avoid the effects of LER. This feature effectively eliminates LER errors by capturing images over a range several microns wide, then averaging measured values over multiple patterns. Moreover, because the images are captured at low magnification with the ACD method, electron beam damage to the resist is also minimized, so obtained measurements exhibit excellent repeatability, high throughput, and minimal damage (see Fig. 9). This measurement method enabled reliable and high stable process monitoring.

3D Structure Measurement

In semiconductor process measurement, there is a growing need to evaluate pattern 3D structures along with planar dimensions. This is because the pattern cross-sectional profile affects device characteristics and yield, and is also an effective measure for assessing process changes. Currently it is not easy to perform non-destructive measurements of 3D structures on actual sample patterns because OCD (optical critical dimension) measurements require special dedicated patterns and AFM (atomic force microscopy)[3] involves contact with the samples.

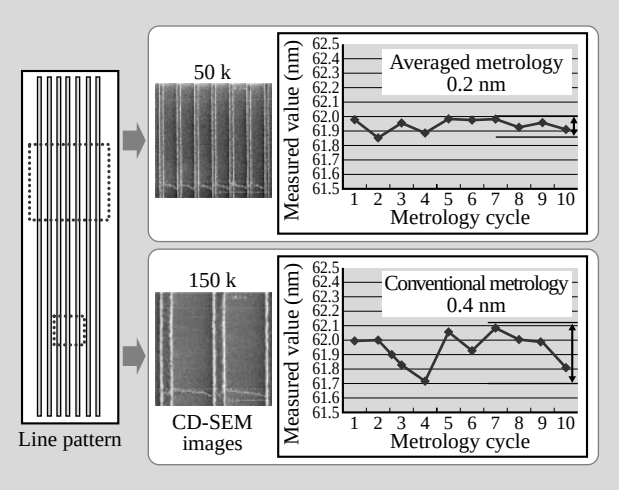

Fig. 9—Effectiveness of Averaged CD Measurement Method. Conventional methods are capable of reaching a metrology variation of 0.4 nm, but the ACD (averaged CD) metrology function reduces this figure to 0.2 nm.

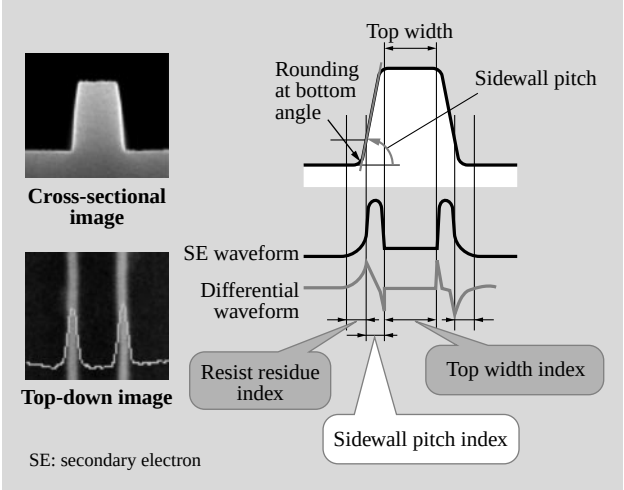

Fig. 10—Deriving Cross-sectional Profile Characteristics by MPPC (multi parameter profile characterization). 3D structural information can be obtained from top-down images.

Hitachi's CD-SEM model S-9380*II* employs a SEM image (top view) as a cross-sectional profile monitoring function, and while analyzing the pattern profile luminance and developing a 3D image profile, an MPPC (multiple parameter profile characterization)[4] monitors for changes in the cross-sectional profiles at the various sites (see Fig. 10). The CD-SEM model S-9380*II* also features a beam tilt observation function for monitoring more detailed pattern cross-sectional deformations. This function involves acquisition of a tilted view of patterns rather than the usual top view by turning the electron beam that irradiates the wafer at an angle. This permits observation of pattern sidewalls and other 3D structures.

DESIGNGAUGE SYSTEM BASED ON DESIGN INFORMATION

As lithographic features have continued to shrink and OPC has become more complex, new requirements have emerged: in fabrication processes the great proliferation of sites that must be measured and monitored and the ability to deal with systematic defects that have coordinate information. To deal with these new concerns, Hitachi developed a measurement method based on design information. Bringing this new system on line has tightened cooperation between the Design Division and the Manufacturing Division in dealing with problem issues, thus permitting much easier modification and adjustment of designs which have improved development efficiency and production yields. In this section we take a closer look at DesignGauge, the system based on this technology that uses design information.

OPC Calibration

OPC is essential in lithography when transferring the design pattern to the wafer. When transferring a pattern, the pattern proximity effects become increasingly pronounced the closer one comes to the resolution limits of the lens, and very complicated techniques are required to correct the problem. There are essentially two kinds of OPC calibration: rule-based OPC and model-based OPC. In the former rule-based OPC, patterns are corrected by extracting patterns by pattern calculations based on correction rules, and this approach is best suited to relatively simple corrections. The latter model-based OPC is better suited for more complicated corrections, and is primarily used in 90-nm node technology and beyond. Fig. 11 depicts the processing flow of the model-based approach. In this method, the generation of an accurate model holds the key to improved OPC accuracy. Note that in both rule-based and model-based approaches, transferring test patterns and acquiring significant amounts of data used for calibration are required, so automated CD-SEM metrology recipe generation is very much desired. After subjecting the device pattern to OPC calibration based on the model, ORC (OPC rule check) is done to verify the appropriateness of the corrections. In the actual calibration process, hot spots—places or sites that are especially vulnerable

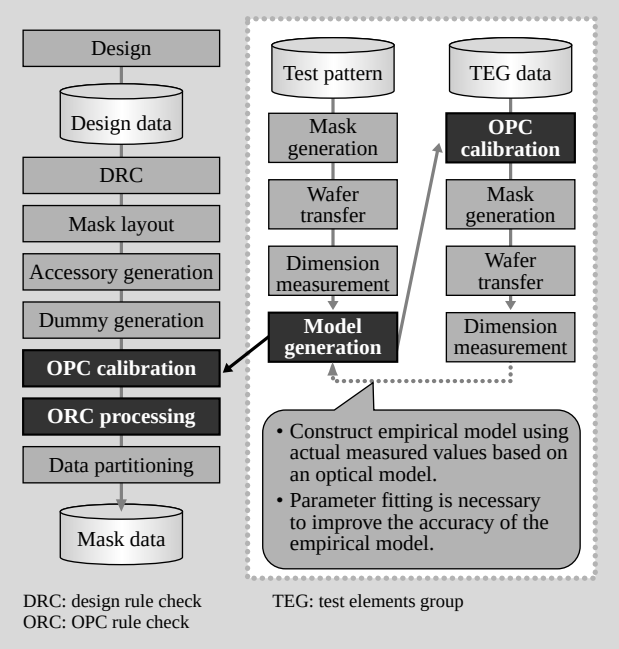

Fig. 11—Model-based OPC Calibration Flow.
Generating an accurate model is the key to improved OPC accuracy.

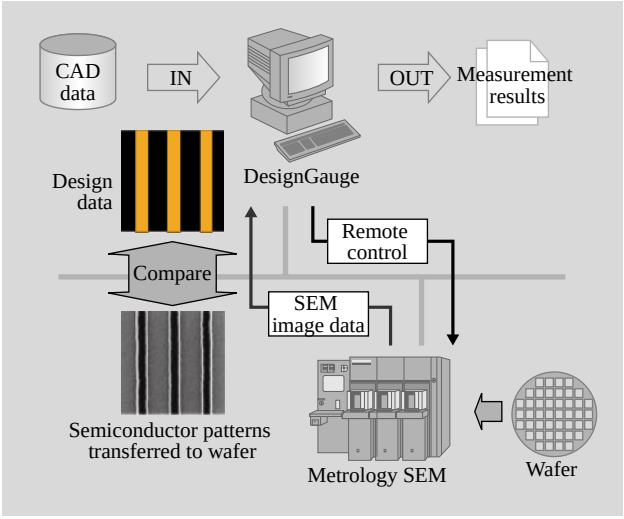

Fig. 12—Main Characteristics of DesignGauge.
The system verifies and compares semiconductor patterns transferred to a wafer against design data with great accuracy.

to pattern variation and deformation—are identified. These sites are monitored during actual processing and the mask may even be modified if it is found to be responsible for reduced yields. Defects in this approach are effectively prevented based on coordinate information and management of sites that are identified in advance as potentially vulnerable hot spots.

Overview of DesignGauge

In the design information-based metrology system DesignGauge, the key to enhanced OPC accuracy is the acquisition of an enormous amount of data for creating the OPC model. This is also very effective for identifying hot spots that in actual processes are vulnerable to pattern deformation[5].

DesignGauge verifies and compares the semiconductor pattern that has been transferred to the wafer against the design information with a high degree of precision. DesignGauge runs on a Windows* OS PC, and is connected to the metrology SEM over the network and to the overall system. This permits automated measurement and metrology recipe generation based on effective use of the design information. Having presented an overview of DesignGauge, let us next examine the main features of the system that are shown schematically in Fig. 12.

(1) Off-line recipe generation

By utilizing CAD (computer-aided design) data, the system is able to generate metrology recipes that in the conventional approach required use of a metrology SEM, but DesignGauge is capable of generating metrology recipes off line.

(2) Remote control

Metrology SEM is controlled remotely when recipes are generated by DesignGauge. SEM image data is acquired from the measurement points specified in the recipe while verifying and comparing the semiconductor pattern against the CAD data. Images acquired in the process are stored in DesignGauge.

(3) Metrology based on CAD data

In addition to the metrology functions available on conventional metrology SEM systems, DesignGauge has the ability to measure the differences between CAD data and actual semiconductor patterns.

(4) Remeasurability

Using the SEM image data stored in the system, DesignGauge has the ability to remeasure device features.

Results of Using DesignGauge

Introduction of DesignGauge has resulted in a great reduction in the time required to generate automated recipes. Specifically, it streamlines the work of acquiring vast amounts of data needed to generate the OPC calibration model, so a process that used to take sometimes well over a month can now be accomplished

*Windows is a registered trademark of Microsoft Corporation in the U.S. and other countries.

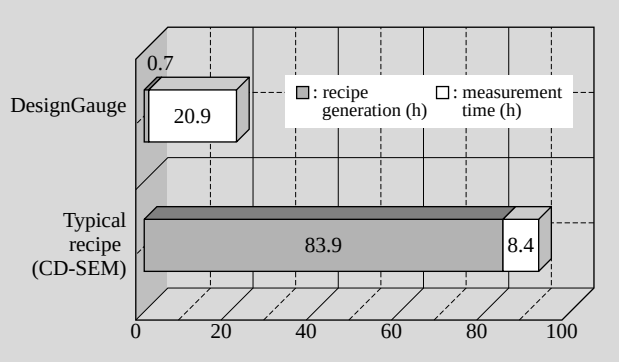

Fig. 13—Effects of Deploying DesignGauge.
Work involved in acquiring huge amount of data used to generate the OPC calibration model is greatly reduced.

in about one week. Fig. 13 compares the efficiency of DesignGauge and the conventional approach in terms of worker-hours for acquiring OPC calibration data from 5,000 points on the surface of a wafer. The conventional CD-SEM is capable of getting the job done, but one can see that DesignGauge is far faster at generating metrology recipes. Dedicated time needed to run the metrology SEM tool is thus significantly reduced.

Going beyond recipe generation based on design information, we plan to push further to achieve even more accurate pattern verification, firmly establish 2D (two-dimensional) design using CAD data, and improve the value-added features of metrology SEM.

CONCLUSIONS

This article described some of the latest metrology technologies to address the needs of advanced semiconductor process measurement.

There is no telling where the relentless trend toward ever-smaller lithography features will end. It is desirable and indeed necessary for inspection and measurement technologies to continue to evolve apace in order to keep up with the continued reduction of minimum device dimensions. Improved resolution and repeatable accuracy go without saying, but the transition from 2D pattern measurement to 3D pattern measurement is essential in order to accurately represent the ever-finer and more complex feature patterns on LSI devices in the years ahead. In addition, measurement technologies based on design information are also necessary to support greater precision and more efficient complex OPC calibration. Ways to support smooth and efficient network management of a full range of inspection and measurement data remain a fundamental issue, and development of inspection and measurement tools that support DFM (design for manufacturability) is an important issue for providers of this type of equipment and tools. Hitachi High-Technologies Corporation remains committed to the development and deployment of measurement technologies that meet these needs.

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