Failure Analysis System for Submicron Semiconductor Devices

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OVERVIEW: Failure analysis of semiconductor device is becoming increasingly difficult as VLSI technology evolves toward smaller features and semiconductor device structures become more complex. Especially considering that the defective area obtained through diagnosis pin-pointing faulty sites is not the same size as the area subjected to physical analysis, and this disparity becomes more pronounced as feature sizes shrink. This prompted us to develop an extremely fine scaled SEM mechanical probing system permitting identification of minute fault sites. The development involved a number of related projects including investigation of a precision probe and stage mechanism that can deal with submicron semiconductor devices, a six-probe mechanism for expanded capabilities of performing inverter measurements and precision single transistor measurements, a probe and sample exchange mechanism that works while under vacuum to achieve high throughput, and a robust CAD navigation system. The system is now ready and available for practical application to 65-nm feature devices, and can be readily adapted to at least the next couple of generation nodes.

INTRODUCTION

FAILURE analysis in semiconductor manufacturing plays a critically important role in shortening the time to get new semiconductor device processes up and running as well as in maintaining satisfactory yields as the part goes into mass production. But it is becoming increasingly difficult for failure analysis—quickly locating and identifying the cause of defects—as semiconductor device structures become more complex and feature sizes continue to shrink to satisfy the rapid advances in functionality and performance of submicron feature semiconductor devices.

Failure analysis is usually done after testing or reliability testing, but as semiconductor device features have continued to shrink even a minute variation in feature geometry can cause a defect, and as ever more

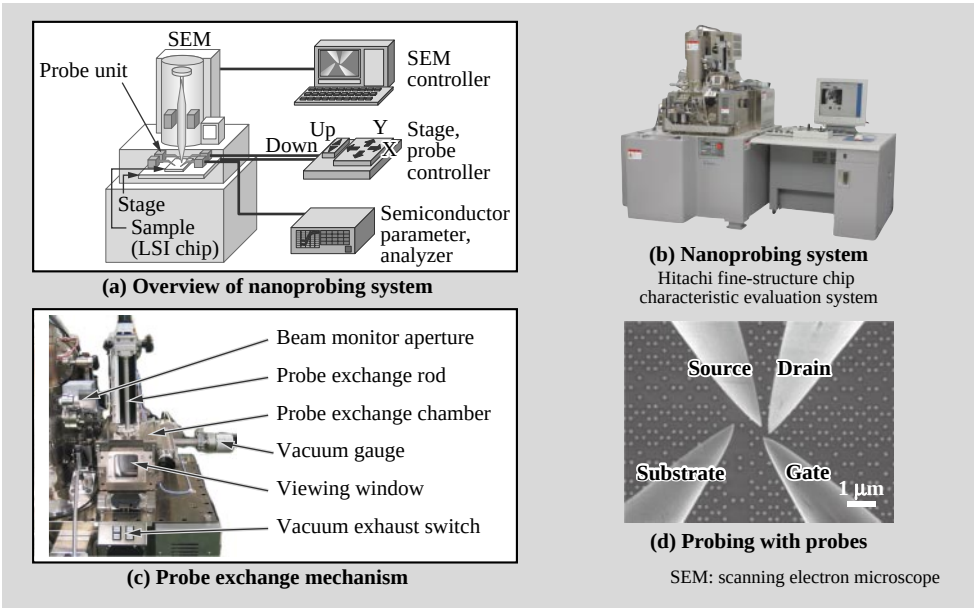


Fig. 1—Submicron Semiconductor Device Failure Analysis System. While observing semiconductor device patterns with an FE-SEM (field-emission scanning electron microscope), the system uses a nanoprobe with 100-nm tip to evaluate single transistor characteristics and wiring resistances by touching a contact or wiring.

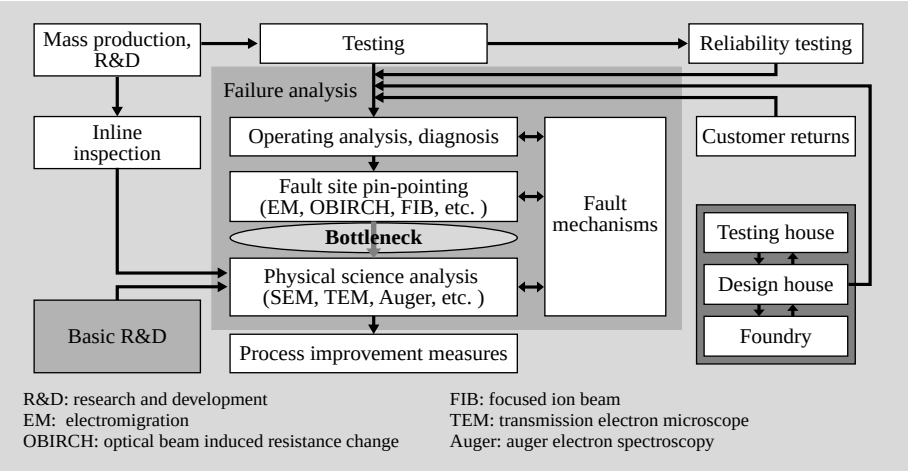


Fig. 2—LSI Failure Analysis Flow. It becomes increasingly difficult to identify fault sites as semiconductor device features continue to shrink, thus increasing the need for such capabilities.

complex semiconductor device structures and new materials continue to emerge, the probability of defects occurring inevitably increases as does the number of chips that need to be analyzed. We are also seeing a growing number of chips being returned by customers as the standard and expectation of semiconductor device reliability continue to increase. Faced with these challenges, failure analysis is becoming increasingly difficult, both qualitatively and quantitatively. One factor compounding the difficulty of failure analysis is the bottleneck between identifying fault sites and physical analysis. Even when the defect can narrowed down to the faulty cell level by diagnosis and fault site pin-pointing, since a cell is typically made up of multiple transistors and interconnections it is difficult to specify through the actual physical analysis exactly which transistor or gate, source, drain, contact, via, etc. should be examined (see Fig. 2).

One solution that has drawn a lot of interest is nanoprobing, a technique involving a minute nano-prove that is brought into direct contact with the circuit and is thereby able to estimate the electrical characteristics of transistor or even smaller feature. This method not only identifies the defective sites, it also characterizes the cause of the defect from the electrical characteristics. Since this narrows down the range of phenomena that must be considered by the physical analysis, it accelerates the failure analysis and improves reliability. A number of nanoprobing system for analyzing LSI faults have been proposed including systems based on SEM (scanning electron microscope), AFM (atomic force microscopy), and FIB (focused-ion beam) technology[(1)–(4)]. This article describes a SEM-based nanoprobing system that provides the same degree of flexibility and ease-of-use as conventional optical manual probes that are used extensively today for LSI failure analysis.

SEM-BASED NANOPROBING SYSTEM: ISSUES AND SOLUTIONS

SEM Resolution and Acceleration Voltage

The essential role of the SEM is to provide the eyes of SEM-based nanoprobing system when probing submicron target sites. This means that the resolution must continue to improve as the IC (integrated circuit) features shrink. And because the objective is to measure the electrical characteristics of the chip, the electrical characteristics cannot be affected or changed by the electron beam emitted from the SEM. To minimize damage to the IC caused by the electron beam, it is essential to reduce the acceleration voltage as much as possible (see Fig. 3). Especially where submicron feature chips and SOI (silicon-on-insulator)

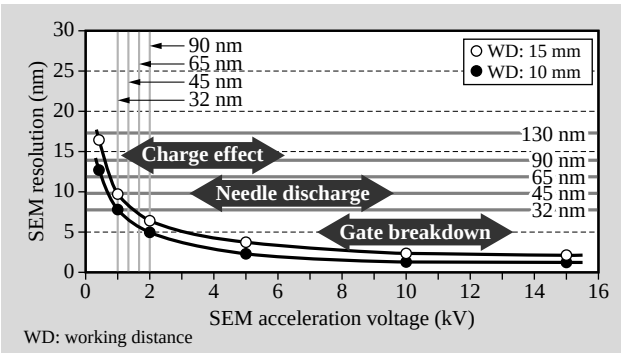


Fig. 3—SEM Resolutions and Acceleration Voltages Required over Next Few Node Generations.
Acceleration voltage must be reduced as IC dimensions shrink to enable improved SEM resolution and reduced damage to the chip.

chips are involved, there is a definite tendency for the electrical characteristics to be affected by build-up of charge on the chip. When faults occur due to residual charge on the chip, precautions are necessary to ensure that the electron beam does not change the electrical characteristics.

A nanoprobing mechanism is inserted between the SEM column and the sample, so a longer working distance is required compared to an ordinary SEM, and this means that the resolution of the SEM is reduced at the same acceleration voltage. But because the acceleration voltage must be minimized, the nanoprobing system must have the same level of resolution as a high-performance SEM for materials observation in order to obtain the required resolution. In this system we were able to realize the desired resolution for a working distance of 10–15 mm which was just enough to install a minute probing mechanism, and we adopted a CFE (cold field emission) source to reduce the amount of electron emissions. Finally, we mounted multiple detectors to ensure no loss of image quality even though the amount of emitted electrons was reduced.

Sample Surface Contamination by Electron Beam Emissions

In SEM, carbon system contamination from electron beam emissions sticks and accumulates on the sample surface. Fig. 4 shows examples where 2 probes measure resistance of a metal plate irradiated by an electron beam in a vacuum of 10^{-3} Pa, a typical vacuum for SEMs. One can see that the resistance varies greatly with the observation magnification and irradiation time that depend on the cleanliness of the metal plate, the concentration of electron beam emissions, etc. Note too that the resistance is far greater at the edges of the irradiated area than in the center. Assuming a transistor that operates at 1–2 V and has a drain current (I_d) of 100 μA, once the contact resistance exceeds 1 kΩ, the adverse effects on the drain current start to become significant. The lower the contact resistance the better when measuring the resistance of substrate contacts, interconnections, and vias, and it is necessary to at least reduce the contact resistance to 10 Ω or lower. Assuming a probing time of about 10 minutes at a measurement site, this yields a value not too far from the required resistance even in the center of the irradiated area.

Because observation magnification increases as device dimensions shrink, contact resistance also increases. In order to reduce this resistance, contamination in the vacuum must be decreased. While it is important to keep the sample chamber at a high vacuum, if the vacuum is increased, this increases the time required to exchange the samples and probes. In this system we have managed to keep the sample surface exceedingly clean by carefully managing the surface processing in the sample chamber, the quality of the wiring, by optimizing the exhaust system, and controlling the chemicals used in the sample preprocessing, so we have succeeded in reducing the contact resistance to about 10 Ω over sufficient long period to perform probing at a pressure of 10^{-5} Pa.

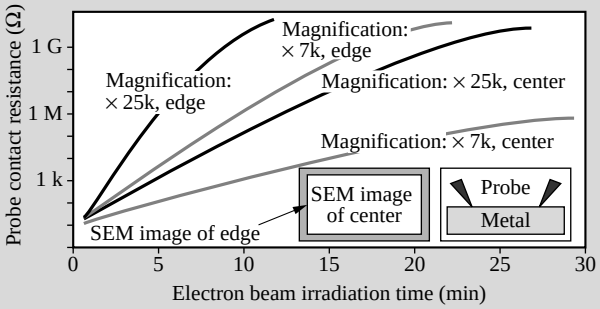


Fig. 4—Electron Beam Emissions Cause Probe Contact Resistance to Change.
One factor preventing the reduction of probe contact resistance is surface contamination. Surface contamination in SEM usually depends on electron beam irradiation time and the observation magnification.

Probe and Sample Exchange

Since measurement is done under vacuum with the SEM-based probing system, achieving a practical level of throughput looming as a major challenge because exchanging probes and samples is a complicated task and takes time. The probes in particular have to be further miniaturized as chip dimensions shrink, and since the life of a probe is fairly short, the ability to quickly and easily change out the probes was absolutely essential. To solve this issue, we adopted a load lock chamber scheme for exchanging probes and samples while maintaining vacuum [see Fig. 1(c)]. Extra probes are stored in the load lock chamber so when needed they can be brought into the measurement chamber by the probe handler and mounted onto the probing mechanism. This approach permits six probes to be changed and vacuum achieved in under 10 minutes by opening and closing a valve, performance levels that are more then sufficient for practical throughput.

Number of Probes

Increasing the number of probes to six in our new SEM-based probing system also increases the wiring and the size of the probing mechanism, and of course these factors affect the vacuum. The simple resistance or a single transistor can be measured with four probes, but it takes six probes to measure an inverter or to perform the detailed measurement to estimate the effects on an adjacent transistor (control adjacent gate potential). In our system, the probing mechanism is implemented very compactly, and is capable of maneuvering six probes in a vacuum of 10^{-5} Pa.

EVALUATION RESULTS

Probing

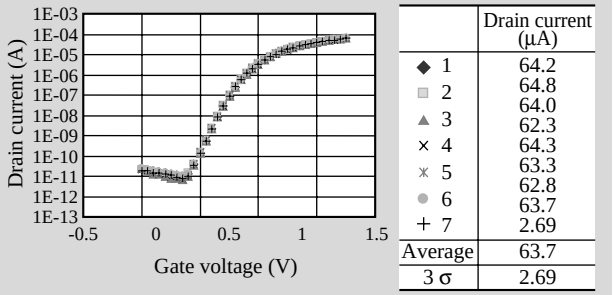
When probing a logic SRAM (static random access memory) implemented in 90-nm process technology with four probes, the radius of curvature of the probe tips is 50 nm [see Fig. 1(d)]. Using narrow or thin probes is not the best choice considering contact resistance and the life of the probes. In order for contact resistance to actually reduce contamination, the probe must be slightly flattened and have a certain degree of thickness. For this study, we applied a probe tip that was of the same diameter as the contact being probed. The contact pitch becomes narrower as chip features shrink, and this complicates the probing. But if the probe is at least as thick as the contact diameter, the system is perfectly capable of dealing with the contact diameter of chip's contact pitch.

Repeatability

It is crucial that measurements performed by the probing system are repeatable. Indeed, the reliability of the fault site data obtained by the system is the key to the system's performance. Fig. 5 shows the measurement results after repeatedly probing the same transistor on a 65-nm feature LSI logic NMOS (negative-channel metal-oxide semiconductor). The variation was 4.2% at 3 σ after probing the transistor 7 times, excellent results considering the extremely small area being probed.

Current Detection Limit

When evaluating a gate dielectric film in low-power-consuming chips, one wishes to measure even very minute quantities current. The main limiting factors on the lower limit of current detection are noise, leakage, and drift. Since measurements are done in a vacuum sample chamber in the SEM-based nano-probing system, noise and drift are relatively good,



	Drain current (μA)
◆ 1	64.2
□ 2	64.8
▲ 3	64.0
× 4	62.3
✳ 5	64.3
● 6	63.3
+ 7	62.8
Average	63.7
3 σ	2.69

Fig. 5—Repeated Probing Time Repeatability.
Measurement reliability is extremely important in failure analysis. In this system data variation affected by the contact of the probe is kept exceedingly small.

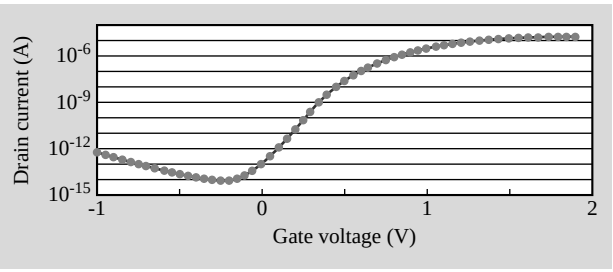


Fig. 6—Current Detection Lower Limit.
Lower limit current measurement is at the fA level, so the system is capable of assessing minute amounts of leakage current.

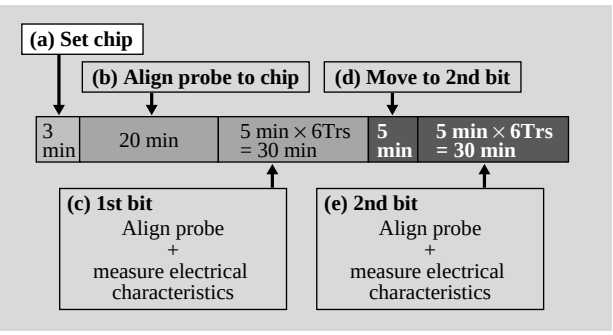


Fig. 7—Average Measurement Throughput for 65-nm Node SRAM.
Should be capable of the same throughput as a conventional optical manual probe.

but we tried to reduce noise even more by strengthening the shielding on the wiring, by reducing the physical oscillations, and by reducing leakage with the use of triaxial wiring. As one can see from the results in Fig. 6, we achieved an excellent lower limit current detection of 10 fA.

Throughput

Improving throughput is another key issue that failure analysis systems must address. As described

earlier, our system supports probe and sample exchanging in the vacuum chamber, very high quality SEM images, and a precision probing mechanism. This combination of features permits handling of images that are equivalent to conventional optical manual probing, so we can expect an equally satisfactory level of throughput (see Fig. 7).

CONCLUSIONS

This paper described the practical development of a SEM-based nanoprobing system that effectively solves the main issues confronting today's LSI failure analysis: increasing complexity of analyzing ever-smaller chips, and the longer times required for analysis.

A key advantage of SEM is that it should be just as easy to use as conventional optical manual probing, so one of our primary objectives was to develop a system that exploits this flexibility and ease-of-use. Development of probe and sample exchanging mechanism under vacuum permits vacuum conditions to be maintained without the user being consciously aware of the vacuum conditions, and the high-quality SEM images and precision realtime probing mechanism will enable direct measurement of actual submicron semiconductor device features.

In terms of measurement precision and throughput, the system is now ready for practical application to 65-nm chips. As VLSI (very-large-scale integration) technology continues to evolve toward smaller features, the basic nanoprober scheme described should remain viable for 45-nm and even 32-nm generation chips, although of course further work will be necessary to reduce the dimensions of the probes and enhance the image quality of the SEM.

Hitachi is committed to further efforts developing and deploying practical nanoprobing systems that will continue to support robust failure analysis as the minimum feature size of semiconductor devices continues to shrink in the years ahead.

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