Vertical Diffusion and CVD Tool for Next-generation Semiconductor Devices

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OVERVIEW: In regard to recent patterns in semiconductor fabrication, two features are clear: mass production of a few product varieties, such as DRAMs and MPUs, or small amount production of many product varieties, such as system LSIs. From now onwards, however, demands for shortening the fabrication period will grow. In the case of large batches (processing 100 to 125 wafers), the standby time needed for output adjustment gets longer, thereby lengthening the fabrication period significantly. Moreover, on top of increases in gas generation and power consumption, it is also a problem that the quantity of dummy wafers consumed in making up for several defective wafers also increases, and the CoO rises dramatically. In response to these challenges, aiming at higher productivity, Hitachi Kokusai Electric Inc. has developed a vertical-type diffusion and CVD tool—called "QUIXACE"—for handling "quick turnaround time" with good process performance at high throughput. With this tool, we will further contribute to improving the production of semiconductor devices.

INTRODUCTION

AS for the recent trend concerning semiconductor fabrication, the shortening of fabrication work periods for mass production of a few product varieties, such as DRAMs (dynamic random access memories), MPUs (microprocessing units), and flash memories, is being strongly promoted. In line with this trend, Hitachi Kokusai Electric Inc. has developed and commercialized a new tool—called "QUIXACE"—incorporating QTAT (quick turnaround time) technology for shortening the cycle time of conventional equipment for handling 300-mm-diameter wafers (see Fig. 1). Moreover, by applying the QTAT technology to its unique vacuum load-lock equipment and creating a series of QUIXACE units, it is possible to improve productivity, and QUIXACE-L/L for handling applications that require interface control (such as controlling oxygen atmosphere and water concentration) was developed and is currently being deployed.

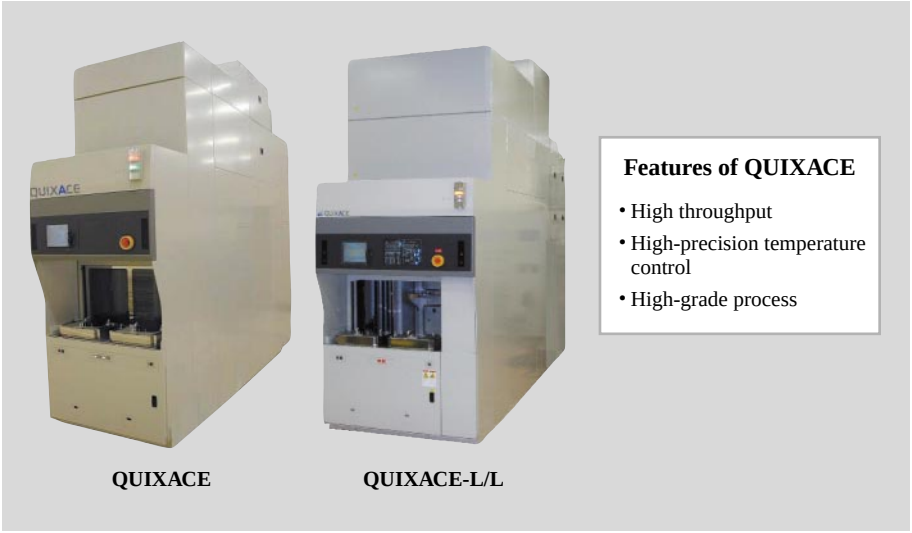

Fig. 1—CVD (chemical vapor deposition)/vertical-diffusion Apparatus "QUIXACE" for Next-generation Devices.
Hitachi Kokusai Electric Inc. has developed "QUIXACE"—based on its amassed extendible high-cleanliness technologies (organic and metallic contamination reduction) for next-generation devices and oxidation-diffusion and gas-phase-reaction technologies—for fulfilling the need for flexibility and high throughput covering small lots up to large lots of 50 to 125 wafers.

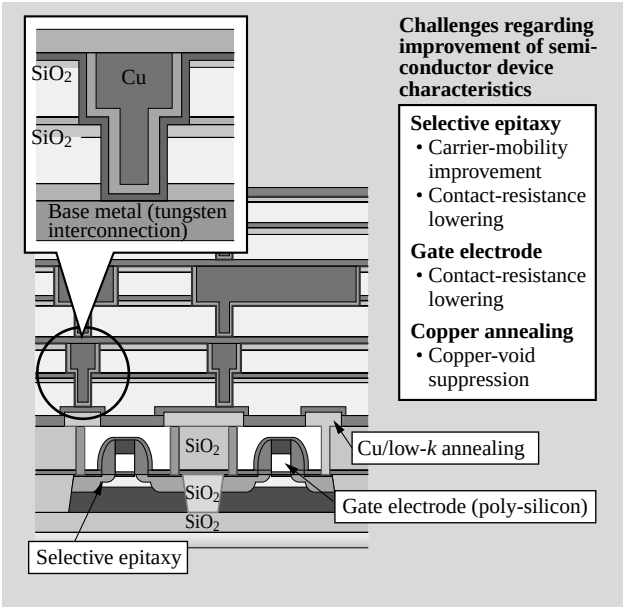

Fig. 2—Structure of Semiconductor Device.
An example structure of a logic system LSI device is shown.

	2003	2004	2005	2006	2007	2008
Technology node	90 nm		65 nm		45 nm	
GOI surface metal concentration (E10 atoms/cm^2)	0.5		0.5		0.5	
Other surface metal concentration (E10 atoms/cm^2)	1.0		1.0		1.0	
Interface carbon concentration (E13 atoms/cm^2)	1.8	1.6	1.4	1.3	1.2	1.0
Interface oxygen concentration (E13 atoms/cm^2)	0.1	0.1	0.1	0.1	0.1	0.1

With scaling-down (to the 45-nm node), cleanliness improvement and interface-control techniques must be established.

(2007 desired value)
- Interface carbon concentration < 1.2E13 (atoms/cm^2)
- Interface oxygen concentration < 0.1E13 (atoms/cm^2)

Source: ITRS 2004 (1)

Fig. 3—Requirement Trend Regarding Wafer-interface Cleanliness.
Forecasted contamination level of wafer surface, which influences device characteristics, is shown.

In the rest of this paper, the development concept behind the QUIXACE series is explained, and the performance and advantages of this series of tools are described.

NEEDS REGARDING SEMICONDUCTOR FABRICATION EQUIPMENT

In regards to semiconductor devices beyond the 90- and 65-nm technology nodes, along with scaling-down and mass integration, high-reliability and high-grade wafer-processing technologies are being sought after.(1) As for device structure, efforts aimed at various configurations such as multi-electrodes are being made, and development of deposition systems that can handle these processes is thus becoming necessary (see Fig. 2).

In addition to introduction of strained-silicon and SOI (silicon-on-insulator) techniques, high-*k* (high-dielectric constant) materials—for lowering leakage current of gate insulator films—are being adopted. Furthermore, to reduce contact resistance of gate electrodes, the demands for reducing impurities on a wafer surface (boundary) are growing stronger year by year (see Fig. 3).

In the case of high-end processing, to reduce conduction faults in copper interconnections, it is necessary to reduce minute foreign bodies and voids—that is, suppress natural oxidation and reduce contamination concentration.

As regards the equipment market for processing 300-mm wafers, along with variation in device structure and handling new materials such as low-*k* and high-*k* dielectrics, the transition to single wafer processing machine that can suppress impurities at the wafer boundary is predicted. On the other hand, reduction of organic and metallic contamination in a vertical-type machine and establishment of high-cleanliness techniques for the wafer boundary have made it possible for a high-productivity vertical-type QUIXACE to also handle these needs.

In addition, by handling rapid increases and decreases in temperature, QUIXACE decreases thermal budget, thereby curtailing the advantage of a single wafer processing machine.

DEVELOPMENT CONCEPT BEHIND QUIXACE

Features of QUIXACE

By applying QTAT technology to our conventional successfully performing large-batch tool (for processing a maximum of 125 wafers) and mini-batch tool (less than 50 wafers) to create a series of machines, we have developed QUIXACE for meeting various user needs—up to production conditions such as atmospheric control and number of processed wafers. By utilizing the following main features—

TABLE 1. QUIXACE Lineup
The lineup of QUIXACE CVD combustion/diffusion machines aimed at next-generation devices is shown.

Process	Machine	Features
Oxidation/LP-CVD	Atmospheric air/nitrogen purge Heat-treatment device	High throughput QTAT production handling
Copper/low-*k* annealing	Load-lock style Heat-treatment device	High throughput Low-temperature control
Side wall Etch stopper	Batch ALD device (low-temperature nitride film)	Low-temperature process High-quality deposition
Wafer fabrication (annealing)	High-temperature-annealing device	High throughput Slip-free
Silicon Strained-silicon formation	Batch Epitaxial-SiGe device	High cleanliness High-throughput-deposition capability

LP-CVD: low-pressure CVD
QTAT: quick turnaround time
ALD: atomic layer deposition

(1) high-precision temperature control,
(2) high-grade processing,
(3) cleaning technology, and
(4) high-speed transfer technology
—QUIXACE dramatically reduces processing time and accomplishes good process uniformity.

Features of QUIXACE-L/L

For film deployment of a load-lock device, copper annealing, gate electrode (poly-silicon), and selective Epi (epitaxial) are available. As a result, a load-lock device "QUIXACE-L/L"—featuring supreme technologies such as cleaning and interface-impurity reduction—was added to the lineup.

Since the main features of QUIXACE-L/L are:
(1) cleanliness-assuring technology,
(2) elimination and control of natural oxide films, and
(3) low energy consumption,
it can be applied to high-grade wafer processing of the next generation.

QUIXACE Lineup

Typical semiconductor fabrication processes and the features of the corresponding machines are listed in Table 1. Adding to a conventional oxidation/diffusion CVD (chemical vapor deposition) unit, the QUIXACE lineup was developed for handling next-generation devices by providing ALD (atomic layer deposition) and selective epitaxial SiGe fabrication.

Under the situation of widely diversified specifications required for machines—such as a batch ALD unit capable of film processing at the atomic level, a high-temperature-annealing unit, and a batch epitaxial-SiGe processing—according to applicable devices, a lineup for handling production of various devices was created by standardizing a platform of machines covering options for handling various devices.

TABLE 2. Basic Performance of QUIXACE
The performance of QUIXACE MINI (50-SiN-wafer oven treatment) is shown.

Item		Specification	Comments
High-precision temperature control	Temperature stability	± 0.5°C	
High-grade process	Transfer-room oxygen concentration	< 20 ppm	
	Film-thickness uniformity	± 0.75%	
	Particles	< 50 pcs	
	Metal contamination	< 5E10 atoms/cm^2	
Cleaning	Maintenance cycle	5 µm	Without purge
		20 µm	With purge
High productivity	Time overhead	45 min	
	Scheduled downtime	< 8%	
	Power consumption	< 70 kVA	

PERFORMANCE AND ADVANTAGES OF QUIXACE

The basic performance of QUIXACE is listed in Table 2.

High-precision Temperature-control Technique

Achieving stress reduction and oxidation suppression for wafers generally involves a sequence for charging a reactor with a boat at low temperature. In

TABLE 3. Basic Performance of QUIXACE-L/L
Exploiting the advantages of vacuum load-lock system to the full extent improves device performance.

Item		QUIXACE-L/L		Comments
		QLV	QLV2	
Processing number (wafers)		100	100	
FOUP opener		2	2	
FOUP stocker		16	16	
Time overhead (min)		266	135	
Nitrogen-exchange method	Transfer-room atmosphere	Air	Nitrogen purge	
	L/L room atmosphere	Vacuum exchange	Vacuum exchange	Vacuum L/L
Hard performance Oxygen concentration (ppm)	In FOUP	Air	< 100	
	Transfer room	Air	< 20	
	L/L room	< 1	< 1	< 0.1
	L/L room (water concentration)	< 1	< 1	< 0.5
Process performance	Metal contamination (atoms/cm^2)	< 1E10	< 1E10	
	Interface oxygen concentration (atoms/cm^2)	< 1E15	< 1E13	Interface control

FOUP: front-opening unified pod L/L: load lock

accordance with this sequence, since it is required to control increases and decreases in heater temperature precisely, a heater mechanism for rapid heating and cooling was optimized, and temperature-measurement and control times were shortened, while temperature stabilization time was shortened. Furthermore, in comparison with a conventional temperature-control mechanism, utilizing our own automatic temperature-control technology dramatically improved temperature convergence after raising heater temperature.

The atmosphere of the transfer room (in the wafer-transportation area) can be controlled to below the 20-ppm level by applying a nitrogen-purging configuration.

Coating Technology

(1) Film-coating uniformity

Introducing an in-plane temperature-control method has attained in-plane uniformity of ± 0.75% in the case of processing 50 Si_3N_4 films.

(2) Metallic contamination

Together with creating metal-free reactor structural materials without limitations, optimizing the gas flow reduces diffusion of heavy-metal ions to the wafer surface.

(3) Maintenance cycle

By controlling reaction-tube temperature while purging, generation of particles is suppressed. By introducing this method, the maintenance cycle is stretched to 20 μm.

Cleaning Technology

As regards CVD machines for 300-mm wafers, owing to the size scaling-up of the reaction tube, operability and excessive time are major challenges facing conventional wafer cleaning. As a result, improving maintainability is important, and development of gas cleaning for mass production is necessary. QUIXACE is equipped with gas-cleaning technology optimized for each application; downtime for cleaning is thereby reduced and high throughput is attained.

High-speed Transportation Technology

By adopting structural parts and technology for a high-speed transfer system, transfer times have been significantly reduced. In the case of a fabrication line for 300-mm wafers, mini-environment compatibility using a FOUP (front-opening unified pod) and automation are becoming mainstream. QUIXACE is a system for complete automation, and the input/output ports of its FOUP (in the interface unit) are compatible with AGV (automated guided vehicle) and OHT (overhead hoist transportation) systems, and satisfy the standard specifications and safety specifications.

Technologies for Establishing Dominance of Load-lock Equipment

The basic performance of the QUIXACE-L/L system is listed in Table 3.

(1) Techniques for creating high cleanliness level

By isolating the atmosphere in the load-lock chamber as well as the boat-elevator structural parts, boat rotating structural parts and associated cables and sensors, a clean load-lock chamber is created.

(2) Technique for controlling impurity concentration at the wafer interface

(a) Natural-oxide-film suppression

A nitrogen-purging room is set up in the wafer-transfer area, and the vacuum load-lock chamber is set up directly below the reaction chamber, and by significantly reducing the oxygen and moisture concentration in the atmosphere from the charge FOUP to the reaction chamber, formation of a natural oxide film can be suppressed. Moreover, by fitting a rapid temperature rise-and-fall heater, low-temperature loading can be reduced even more.

(b) Elimination of natural-oxide-film

By means of a reducing gas, a natural oxide-film formed on the wafer surface can be removed. And by improving the gas-reduction method, the removal efficiency can be improved, so even more oxide can be removed.

(3) Space saving

(a) "Side-maintenance" free: Access is possible from the front and back of the system. Accordingly, by setting systems up side by side, a floor-space utilization can be cut by 12.5% compared with that taken up by conventional equipment.

(b) Improved maintainability: By adopting a structure that enables parts such as the reaction tube to be inserted and removed from the load-lock chamber, operability is dramatically improved.

CONCLUSIONS

In this paper, a vertical-type diffusion and CVD tool—called "QUIXACE"—for the 65-nm technology node was described. With the scaling-down and further integration of semiconductor integrated circuits, gate insulator films are getting thinner and thinner. As a consequence of this trend, new materials and new film-formation methods must be developed. From now onwards, Hitachi Kokusai Electric Inc. will continue research and development that will make significant contributions to the industry by improving hardware-control technology, process control technology, and equipment maintainability in preparation for the nanotechnology era.

REFERENCE

(1) ITRS 2004: ITRS

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