ULSI Devices: Current Status and Future Prospects of Research and Development

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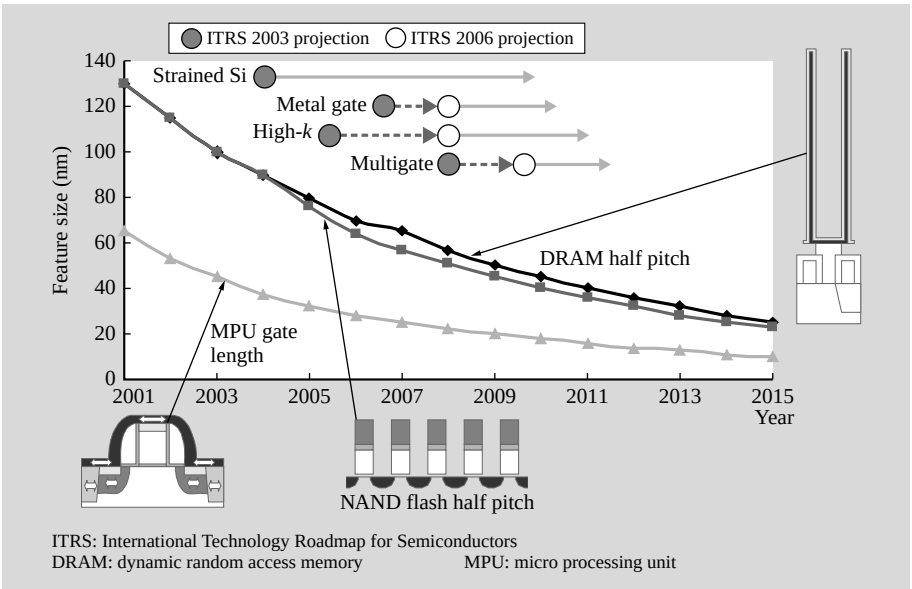
OVERVIEW: Now well into the early years of the 21st century, it has been four years since booster innovations were proposed as a way to extend and sustain CMOS performance gains that until now were achieved by reducing feature size, and development is under way on devices beyond the 2nd generation. Microfabrication development has been largely driven over this period by NAND type flash memory, and the pace of progress exceeded the projections of the ITRS (International Technology Roadmap for Semiconductors). Yet aside from strain engineering, none of the technologies anticipated as boosters are ready for practical implementation, and will not be introduced as anticipated by the ITRS time-line. In this paper we will consider the current status of research and development in 2007 on ULSI devices that defines the development of the latest fab equipment, and the direction this work will take in the years ahead.

INTRODUCTION

THE semiconductor industry that has witnessed such remarkably sustained and rapid growth for more than 40 years is now in the early years of the 21st century beginning to undergo a fundamental change in the way further performance gains will be achieved. To shed light on this development, this paper reviews the current state of research and development as of 2007 on ULSI (ultra-large-scale-integration) processes and devices focusing on CMOS (complementary metal-oxide semiconductor) technology. The 2003 ITRS (International Technology Roadmap for Semiconductors)[(1)] declared that new transistor designs must incorporate booster technologies in order to sustain the performance gains that have been achieved by shrinking transistor geometries in the past. It was anticipated that the booster technologies would be successively incorporated in future ITRS technology nodes beginning in 2006, but it turns out that this time frame was not realistic so we will examine the current development status of these technologies (see Fig. 1).

Here we will consider recent R&D (research and



ITRS: International Technology Roadmap for Semiconductors
DRAM: dynamic random access memory MPU: micro processing unit

Fig. 1—Microfabrication Technology Roadmap.
By using silicon technology for MPU gates, smaller feature sizes are achieved compared to the half-pitch value indicating the overall processing technology level. Beginning in 2005 DRAM was succeeded by NAND type flash memory as the primary driver of microfabrication technology.

development) progress on four key booster technologies: (1) multigate structures, (2) channel strain, (3) high-*k* (high dielectric constant) materials, and (4) metal gates. These last two are sometimes lumped together under the rubric of gate stacks. Next, we discuss shallow junction technology that in the revised 2006 ITRS assessment was highlighted as the technology likely contributing the most to improved transistor performance in the near term future. Finally, we will consider the latest advances in wiring and interconnect technology that plays such a key role in determining the performance of ULSI devices.

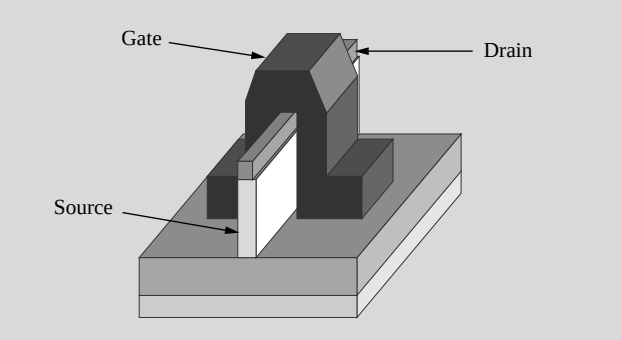


Fig. 2—FinFET Element Structure.
FinFET device structure implemented with multigates.

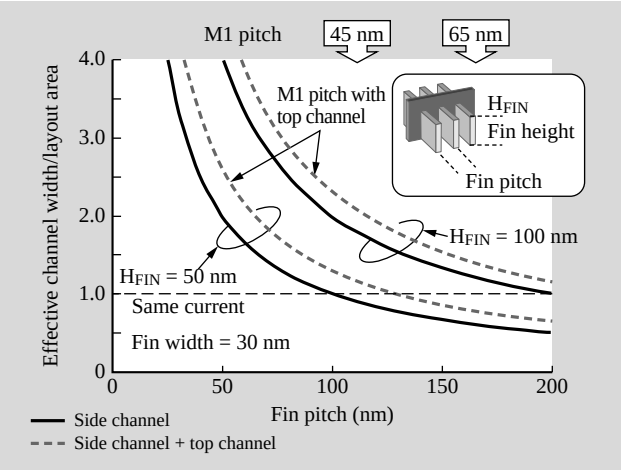


Fig. 3—FinFET Layout, and Comparison of Current Drive with Feature Size as a Parameter.
FinFET exceeding planar MOS (metal-oxide semiconductor) while occupying the same layout area was recently reported.

MULTIGATE MOSFETS

A multigate MOSFET (metal-oxide-semiconductor field-effect transistor) incorporates more than one gate into a single device, and effectively suppresses leakage current in low impurity concentration channels using field effects from the multiple gates to control the channels. This design avoids the deterioration in mobility resulting from high concentration channels as well as GIDL (gate induced drain leakage), so it is anticipated that multigate MOSFETs will boost device performance. Many kinds of device structures have been reported, but now they are conveying on fin-channel based designs proposed by Hitachi: the fully-DELTA (depleted lean-channel transistor)[2], the FinFET (field-effect transistor)[3], and the omega-FET[4]. Significant recent fin-channel device developments include proven enhanced drive capability as a result of dense pitch fins based on improved lithography and dry etching techniques, general capability to form fins using bulk substrate, and better control over threshold voltage variability.

Fig. 2 shows the typical structure of a FinFET element. Because the fin is cut down to the dimension of the thin film to become the channel, the channel width determining the current drive is defined by the height of the fin. This means that in order to enhance the drive capability, it is necessary to fabricate an array of very thin standing fin forms within a narrow pitch. Fig. 3 compares the current drive of the FinFET with a conventional planar device taking feature size and pitch as parameters. A processing technology for both the 65-nm and 45-nm nodes was developed, and a FinFET device that provided better drive than an equivalent planar MOS circuit while occupying the same layout space was successfully demonstrated[5]. The FinFET was initially formed using SOI (silicon-on-insulator) substrate since the thickness of the SOI controlled the height of the fin[3]. However, more recently the ability to fabricate fins using bulk substrate has also become fairly commonplace[6]. This can be attributed to better control in the depth direction based on matureness of CMP (chemical-mechanical polishing) technology.

Concern has largely focused on threshold voltage variability, because this largely defines the scaling limit of bulk MOSFETs. This is because it is generally assumed that variability will increase due to the statistical variability of impurities even if feature size variability is well controlled[7]. Impurity variability is given by

$$\sigma V_{\mathrm{th}} \propto \frac{t_{\mathrm{ox}} N_{\mathrm{A}}^{1/4}}{\sqrt{L_{\mathrm{g}} W_{\mathrm{g}}}}$$

where t_{ox} is the thickness of the gate dielectric film, N_{A} is the channel impurity concentration, and L_{g} and W_{g} are the channel length and channel width, respectively[8]. The FinFET is extremely effective for

suppressing threshold voltage variability because it only requires a channel impurity concentration of about 10^{15} cm^{-3} (versus 10^{18} to 10^{19} cm^{-3} for the conventional CMOS device), and also because, as we mentioned above, the width of the channel can be widened. SRAM (static random access memory) cells based on this technology were successfully fabricated, and variability results were reported(7). Variability has always been a serious problem in the fabrication of SRAMs, so the availability of fin-channel devices should be a major driving force for improving the performance of this type of memory cell.

STRAIN-STRESS EFFECTS

The 2005 issue of the *Hitachi Review* (Vol. 54, No. 1) contained an overview of the then current state of strain engineering. Strain engineering refers to a strategy of deliberately inducing crystalline distortion (strain) in the MOSFET channel, which enhances carrier (electron and hole) mobility and thereby conductivity through the channel. Given the great difficulty of achieving further performance gains in the current generation of CMOS devices by downscaling alone, the industry is optimistically hopeful that strain engineering will break the deadlock and open the way to further performance gains. Indeed, it would be no exaggeration to say the more than half the papers presented at CMOS device and process conferences over the past few years have been related to strain engineering in some way.

The current mainstream approach for inducing strain in CMOS devices is the so called *external stress method* implemented by controlling the production process. Research has been focused on two methods in particular: deposition of an SiN layer applying tension or compressive stress to the top of the gate electrode, or recessing the source/drain region and depositing either SiGe or SiC by selective epitaxy. The earlier approach to strain engineering based on SiGe-containing substrate that was so actively investigated has now all but been abandoned out of concern for substrate cost and crystal defects, and only SSOI (strained silicon on insulator) type substrate is currently regarded as a viable candidate and is being marketed SOI substrate manufacturers. In this section we will discuss the importance of processing technology in external stress.

As one can see in Fig. 4, there is a very close relationship between feature size and the magnitude of stress — that is, the degree to which the performance of the device is improved. For example, in the SiN film stress device shown in Fig. 4 (a), the thickness (A) of the SiN film, height (B) of the gate electrode, and distance (C) from the gate electrode to the isolation region are all critical dimensions affecting the magnitude of the strain. In the SiGe buried device shown in Fig. 4 (b), the depth (A) the Si substrate is recessed, width (B) of the recessed region, size (C) of the undercut, local curvature (D) of the recessed region, and thickness and composition (E) of the epitaxially grown SiGe layer all affect the magnitude of the strain. Si substrate recess processing in particular is entirely dependent on the performance of the equipment, because an etching stop layer or similar technique cannot be used in this case. A recent article in the 2006 issue of *Hitachi Review* (Vol. 55, No. 2) detailed the growing problem of increased element characteristic variability in the fine-feature CMOS devices, so if characteristic variability is further exacerbated by strain engineering, then it will be very difficult to adopt this technology. In order to reconcile strain engineering with reduced characteristic variability, it is essential to develop technologies for assessing and controlling

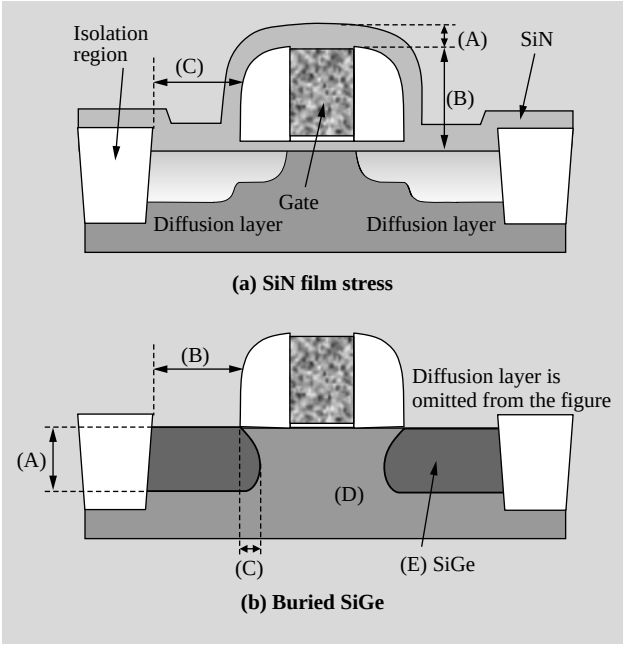


Fig. 4—Dimensions Affecting Stress Magnitude Using External Stress Technology.
In SiN film in (a) stress is affected by thickness (A) of the SiN film, height of the gate electrode (B), and distance from the gate electrode to the isolation region (C). In the SiGe buried device in (b) stress is affected by depth (A) the Si substrate is recessed, width (B) of the recessed region, size (C) of the undercut, local curvature (D) of the recessed region, and thickness and composition (E) of the epitaxially grown SiGe layer.

the critical dimensions listed above. Among the technology booster candidates mentioned earlier, only external stress-induced strain engineering has reached the level of practical implementation. Yet three years have elapsed since strain engineering has been available, and so far the technology has only been incorporated in high-performance MPUs (micro processing units) of a few manufacturers. This is because at the present time only large-scale system chip such as MPUs with the range to absorb performance variability can exploit the advantages of strain engineering. More advanced processing technologies are thus much desired so strain engineering can be applied to a more diverse range of products, including low-power equipment.

GATE STACKS

Structures based on high-*k* gate dielectric film and metal gates instead of polysilicon gates would be highly effective for reducing CMOS OFF leakage while increasing ON current, and is thus one of the most eagerly anticipated technology boosters that have been proposed. Unfortunately, the prospective date for introducing this technology keeps getting put off. Here we present an overview of materials-related research in this area that was conducted up to now.

In the process of selecting high-*k* materials, the thermal stability of binary oxides was investigated[9], the list of candidates was narrowed by examining the thermodynamic stability of the materials, then a small number of candidates was derived based on dielectric and bandgap[10] considerations. Requiring a dielectric constant of more than 10 and a bandgap of more than 5 eV, we ended up with a list of 12 materials: Sc_2O_3, Y_2O_3, EuO, La_2O_3, Gd_2O_3, Ho_2O_3, Er_2O_3, Tm_2O_3, Lu_2O_3, ZrO_2, HfO_2, and Al_2O_3. The rare earth elements exhibit large hygroscopicity, so attention was focused on the group IV oxides (ZrO_2 and HfO_2) and the group III oxides (Al_2O_3 and Y_2O_3). Through actual deposition and analysis of thin films, it was found that ZrO_2 formed silicide at around 900°C. The HfO_2 did not form silicide until 1,000°C, but the crystallization temperature was problematically low at 450–600°C. There has been some discussion of adverse effects using polycrystalline film as a gate dielectric film, but we selected Al_2O_3 — and SiO_2 — doped HfO_2 because we found through our analysis that it maintains an amorphous state even through activation anneal and other high-temperature processes (see Fig. 5). In HfAlO (hafnium aluminate), the relation between the composition ratio of Al_2O_3/HfO_2 and the dielectric constant is nearly linear, and with an Hf composition of about 30%, a dielectric constant of about 15 is obtained and is quite resistant to thermal processing up to a temperature of about 1,050°C[11]. Since Al_2O_3 and HfO_2 can be fabricated as an alternating layered structure, the structures are usually formed by ALD (atomic layer deposition). HfSiO (hafnium silicate) is generally formed by MOCVD (metal-organic chemical vapor deposition) because it does not contain the type

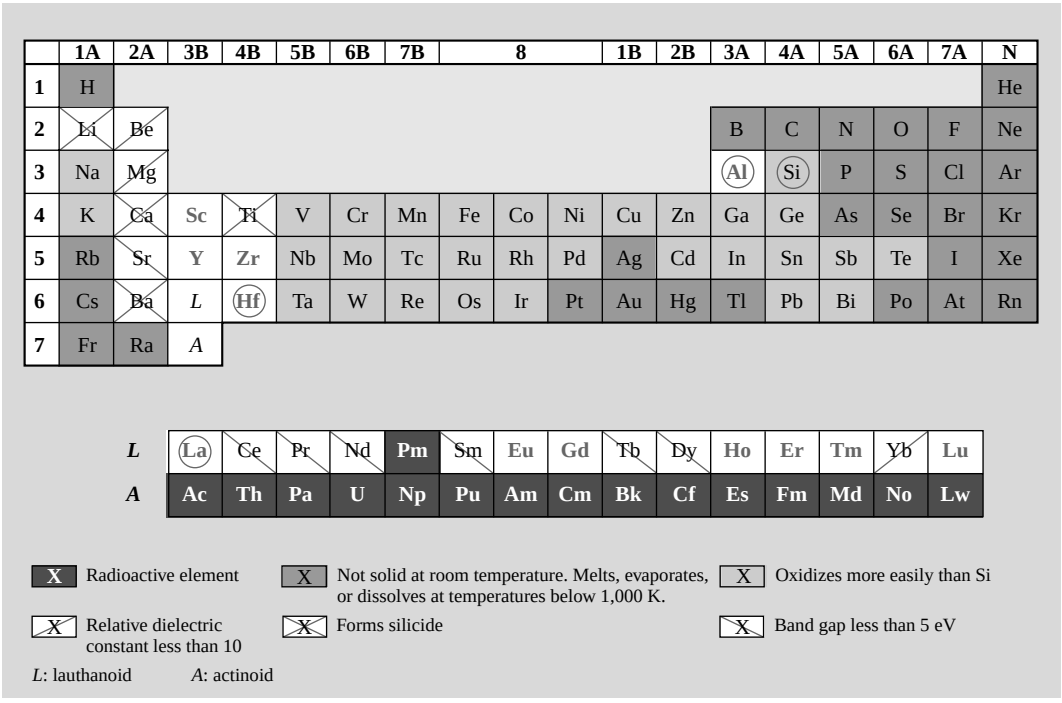


Fig. 5—High-k Material Selection Process. Selection was made based on four criteria: (1) solid at room temperature, (2) is not a radioactive material (prevents soft errors), (3) will not melt, evaporate, or dissolve at device fabrication process temperature [1,000 K (727°C)] and stable on Si substrate, (4) dielectric constant greater than 10 and band gap greater than 5 eV.

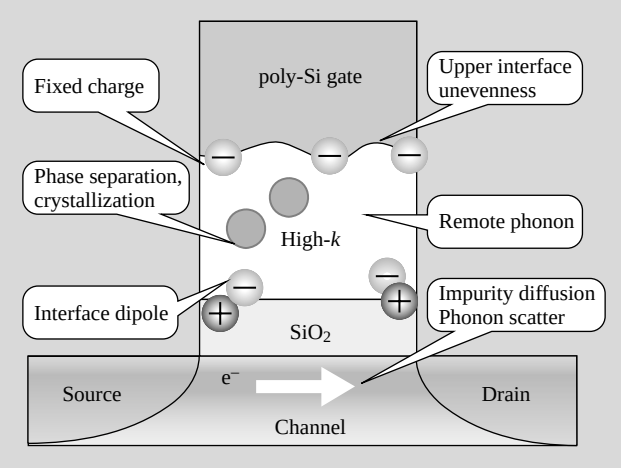


Fig. 6—Cause of Reduced Mobility in High-k Gate Stacks. Model shows the cause of reduced mobility in high-k films.

of oxygen suitable for ALD, but by developing the precursor, we were able to successfully form HfSiO film by ALD.

After developing a short list of materials, it was discovered that diminished mobility and controlling the threshold voltage were formidable challenges to forming high-*k* gate dielectric films. The Hitachi Group then conducted a study, and discovered the factor behind reduced mobility in high-*k* films (see Fig. 6). Armed with this knowledge, we developed an interface nitrogen concentration precision control technology, and demonstrated its effectiveness for suppressing the reduced mobility[13]. Turning next to the threshold voltage control problem, it was realized that if an HfO_2 system is used for the gate dielectric film which causes the pFET threshold voltage to increase above 0.5 V, this cannot be offset by a conventional channel implant. Chris Hobbs et al. conducted a systematic study to find out why, and discovered that the flat band shift does not depend on the thickness of the HfSiON film or on the thickness of the underlying film, so it must be caused by the upper interface[14]. Then K. Shiraishi et al. found that the formation of a dipole at the upper interface cased by electrons moving to the polysilicon side when oxygen deficiency occurs in the HfSiON film was the chief cause of the flat band shift[15]. Exploiting this phenomenon in reverse, Hitachi Group proposed a novel method for increasing the ON current of low-power transistors[16]. From the 45-nm node and beyond, the target EOT (equivalent oxide thickness) is less than 1 nm for logic devices, so the initial investigation focused on lanthanum aluminate, high-dielectric-constant La_2O_3 doped with Al_2O_3[17]. Because the increase in inversion-layer capacitance due to polysilicon electrode depletion (0.3–0.4 nm) cannot be ignored, many have advocated introducing high-*k* film and a metal gate that is not depleted as a set. The big drawback of this approach is that using dual metal gates with different metals for the nFET and for the pFET greatly complicates the processing and substantially increases the cost. To address this problem, Renesas Technology Corp. proposed a method of holding down the process costs while minimizing gate depletion by adopting a poly-Si/TiN deposited metal stack for just the pFET and phosphorus-doped poly-Si for the nFET[18]. To develop a way of implementing both n and p with metal gates, efforts are focused on a FUSI (fully silicided) approach in which the gates are completely replaced by silicide. There is very active research effort under way to determine the work function for n and p through the composition of silicide and segregation effects of pure metal[19]. In addition, a theory was recently proposed describing the effective work function of a metal/Hf system high-*k* dielectric film interface by combining "generalized charge neutrality level" and the oxygen vacancy model[20]. Gate stack design guidelines are emerging based on a combination of metal gate electrode and high-*k* dielectric film.

DIFFUSION LAYER FORMATION TECHNOLOGY

Since further reduction of the gate dielectric is stalled because of the decision to not introduce high-*k* film, attention has turned to diffusion layer formation technology as alternative technology booster for sustaining and extending transistor performance. This is because making junction shallower will increase the effective channel length while suppressing short-channel effects, and decreasing diffusion layer resistance will increase drive current. Here we will examine activation and impurity implant techniques used in forming ultra-shallow junctions, then describe diffusion layer evaluation technologies.

Annealing Technology

Beginning with the 45-nm node, new technologies were introduced for forming diffusion layers. New technologies had to be developed because the low-resistance ultra-shallow junctions required by the CMOS S/D (source/drain) diffusion layer specified by the ITRS (see Fig. 7) simply cannot be created using the conventional spike lamp anneal [spike RTA (rapid thermal anneal)] in combination with ion implantation.

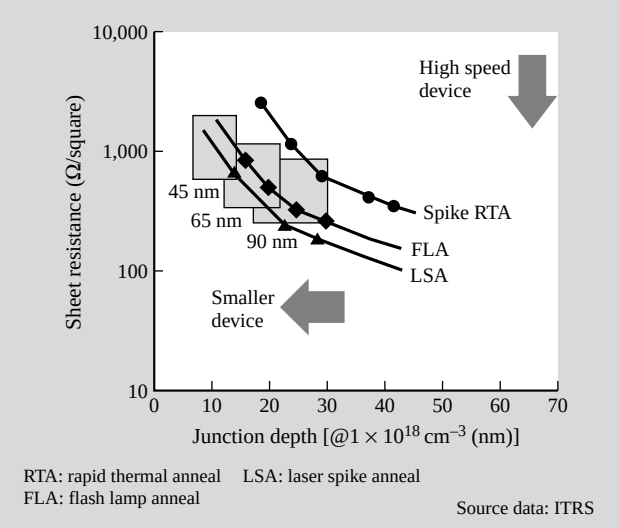


Fig. 7—Diffusion Layer Shift Resistance as a Function of Junction Depth Required by Each LSI Generation. New technologies being considered for forming the diffusion layer for the 45-nm node and beyond.

Basic requirements of anneal processing are *high temperature* and *very short time*, and two new sub-millisecond annealing technologies have been developed that can provide the high temperatures ranging from 1,200 to 1,350°C and the short times ranging from seconds to milliseconds required by the 45-nm node: LSA (laser spike anneal)[21] and FLA (flash lamp anneal)[22]. Transistor threshold voltage is related to effective channel length (L_{eff}), so variability increases as device dimensions decrease. In addition, transistor delay time is strongly dependent on the overlap capacity between the diffusion layer and the gate electrode, and is directly affected by channel length variability. It is generally anticipated that sub-millisecond anneal technology will help control not only downscaling in the vertical direction (i.e. the adoption of shallow junctions), but will also help suppress channel length variability caused by lateral variability of S/D diffusion layer. The new anneal technologies can be simply substituted for the conventional spike RTA in the final process module. The problem is that forming diffusion layers for the 45-nm node using just the sub-millisecond annealing technologies yields very different impurity profiles around the diffusion layer derived from 90-nm and 65-nm nodes, and this greatly increases the device development time since the profiles have to be reconstructed. The mainstream solutions are to suppress short-channel effects and other lateral diffusion problems by either (1) adopting a finely adjusted halo condition and heavy element such as indium (In) or antimony (Sb), or (2) introducing a secondary dopant to the source/drain diffusion layer such as carbon (C), nitrogen (N), or florine (F), in conjunction with a technology for extending the life of spike RTA, either spike RTA plus LSA or spike RTA plus flash. Note that the improvement in device performance comes not from downscaling but from improving the activation of the gate electrode and diffusion layer impurities by using shorter times and higher temperature anneals by LSA or flash thermal processing.

Impurity Implant Technology

Ion implant energy for forming ultra-shallow diffusion layers can be reduced to under 0.5 keV using light-mass P-type impurity boron (B). But reducing the implant energy also reduces the beam current which causes productivity to fall, and adopting low-speed energy mode creates energy contamination problems. One way to circumvent these problems is to increase the effective implant energy by injecting heavy mass molecular ions such as BF_2. Development of cluster ion implantation is another significant development using decaborane ($B_{10}H_{14}$) or octadecaborane ($B_{18}H_{22}$)[23] as the injection ions. The big advantage of this approach is that the same implant dose can continue to be used even while accelerating the energy and reducing the beam current, so productivity is enhanced and the beam angular spread is restrained. Note that this ion beam angular spread directly affects the variability of transistor characteristics discussed earlier, so it is fundamentally important to restrain this parameter as junctions are made shallower.

Evaluation Technologies

Procedures for evaluating of diffusion layers are broadly divided into two approaches: measuring the sheet resistivity and assessing concentration profiles in the depth direction. A 4-point probe is used to measure the sheet resistance, but as junctions become increasingly shallow, the probe can penetrate through the layer so it has become increasingly difficult to obtain an accurate measurement. This led to the development of a number of new technologies including noncontact measurement using a mercury probe[24] and technology for measuring the contact area or shallow penetration depth using a sub-micron scale probe (see Fig. 8)[25], and these technologies will eventually be used for in-line device evaluation in 45-nm mass production fabs. Turning to the latter approach — assessing concentration profiles in the

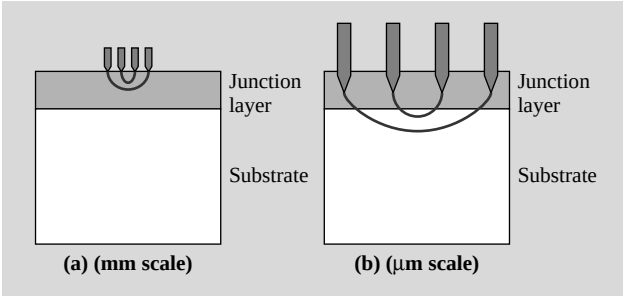


Fig. 8—Schematic of Ultra-shallow Junction Measurement Using a 4-point Probe.
If the gap between probes increases, it becomes impossible to obtain an accurate measurement of the resistance due to the influence of the underlying layer, even when measuring the same junction.

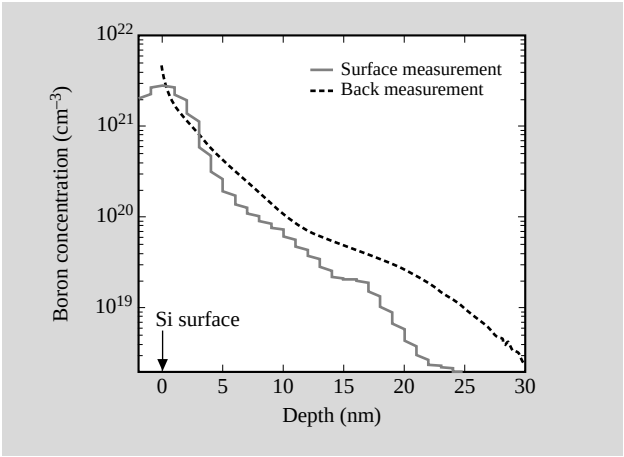


Fig. 9—Boron Ultra-shallow Junction SIMS (secondary ionization mass spectrometer) Profile.
Inaccurate surface measurements are obtained, because the concentration profile near the surface is distorted by one-dimensional element knock-on.

depth direction — the conventional technique of only evaluating one-dimensional concentration profiles in the depth direction by SIMS (secondary ion mass spectrometry) is no longer adequate. This is because, as junctions become shallower and impurities approach the silicon surface, the concentration profile near the surface that is supposed to be measured by the knock-on of the one-dimensional element used in SIMS measurement becomes distorted, thus making accurate measurement impossible. This is because a two-dimensional concentration profile conforming to the structure of the device is required. Because SIMS avoids to be affected by the surface, the practice of performing measurements from the back of the wafer has become widely adopted (see Fig. 9). Research is also focused on developing SSRM (scanning spread resistance microscopy) that combines AFM (atomic force microscope) with a sheet resistance measurement technique to enable observation of two-dimensional concentration profiles of device cross-sections[27]. These metrology techniques still require a very sophisticated level of processing technology, so development of simpler technologies is urgently required.

LSI INTERCONNECT TECHNOLOGY DEVELOPMENTS

MOSFET technology that we have been discussing up to this point is fundamentally important to the performance of LSI devices, but the importance of interconnects — the fine-line metal patterns interconnecting MOSFETs — is increasing rapidly. It has been estimated that close to half the signal delay and power dissipation of logic LSIs for the 90-nm node and beyond can be attributed to the interconnects[28]. In order to restrain signal delay and power consumption, it is essential to reduce interconnect resistance and interconnect capacitance, and hopes are riding on a two-pronged approach involving both materials and processes. Here we present an overview of current interconnect related developments for logic and memory devices.

Logic Device Interconnect Technology

To reduce the interconnect resistance in logic devices, we have already seen a fundamental transition in interconnect metallization from aluminum (Al) to low-resistance copper (Cu) that occurred during the 250-nm to 180-nm generations[29]. Copper interconnects have been standard in logic LSIs since then. Now with Cu interconnects especially after the 45-nm node we are confronted with a new set of issues, most notably how to suppress conducting failures caused by EM (electromigration) and SIV (stress-induced voiding) that occur with increasing frequency as feature sizes shrink. A number of solutions have been proposed, but one of the most promising is to use copper alloy in which the copper is doped with small amounts of a different metal (Mn, Mg, Ni, Al, Ag, and so on) because this would extend the current metallization scheme without greatly modifying the fab processing[30]. Turning to the reduction of interconnect capacitance, this can be achieved by providing insulation between the fine metallization patterns with low-*k* (low dielectric constant) film. The introduction of low-*k* films began somewhat later than the adoption of Cu interconnects, but began to be

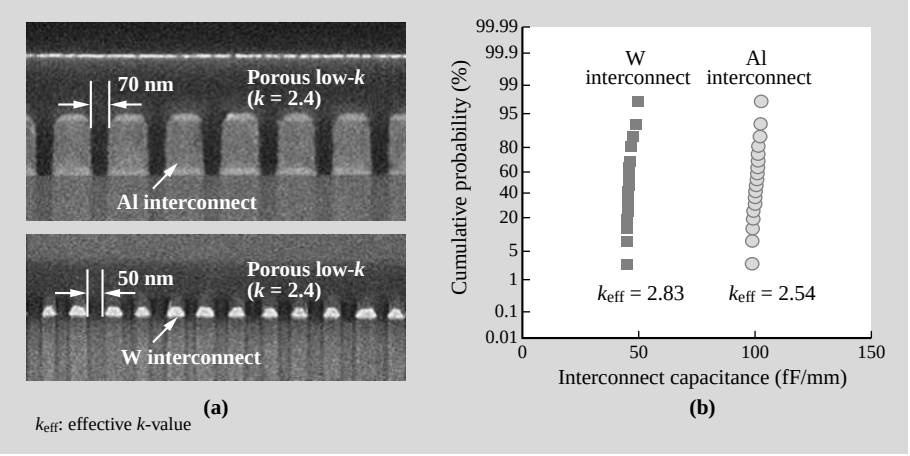


Fig. 10 — Cross Sections of Al and W Interconnects Using Porous Low-k Dielectric Film (a), and Interconnect Capacitance Cumulative Probability Distribution (b). Al and W interconnects buried by spin coated porous low-k dielectric film (k = 2.4) for 50-nm node feature dimensions. Compared to the conventional SiO_2 dielectric film, interconnect capacitance is reduced by more than 30%.

implemented in earnest during the 180-nm to 65-nm nodes when silicon dioxide (SiO_2) (relative dielectric constant k = 4.1) started to be replaced by low-k dielectric films (relative dielectric constant k = 2.7–3.7). Dielectric constant k values must be pushed even lower with each successive generation, and particularly beyond the 45-nm node, the low-k porous dielectric films with a k value of less than 2.5 have emerged as the material of choice to achieve these low levels. The drawbacks of the new porous films is that they do not stand up well to the various low-k dielectric film processes and their dielectric reliability is greatly reduced[31]. Reduced mechanical strength is especially problematic, and the porous low-k films have a tendency to peel or crack when subjected to the major physical stresses of CMP (chemical mechanical polishing) planarization processing and packaging processing. A great deal of work is now being done to address these concerns including the design of stronger low-k porous dielectric films[32] and various techniques using ultraviolet light and electron beams to produce better quality and more robust films[33].

Memory Device Interconnect Technology

In the case of memory devices such as DRAMs and flash memories, manufacturers have deliberately not introduced costly Cu/low-k interconnect processes because of fierce cost competition in the memory sector. Instead there are tenacious efforts to extend the useful life of lower cost Al/SiO_2 metallization, but the limits of this approach are expected to be reached by about the 50-nm node[34]. The first limit is the Al interconnect processing limit. Residue is produced ever more frequently when Al is subjected to dry etching as device dimensions shrink, and this is a major factor in reduced yields. For this reason, Cu interconnects — that raise no concerns about dry etching residue and can better accommodate further scaling — have been adopted in some DRAM products. If concerns about the cost factor can be eliminated, there can be little doubt that Cu would quickly become the interconnect metal of choice in memory devices. The second limit is imposed by the embedding characteristic due to the nature of SiO_2 (silicon dioxide) dielectric films and interconnect capacitance. As the gap between interconnects narrows and the aspect increases, the conventional plasma-enhanced SiO_2 deposition method becomes unable to bury the interconnects, and the interconnect capacitance increases beyond tolerable levels. To address this problem, Hitachi, Ltd. and Hitachi Chemical Co., Ltd. teamed to develop a coating type porous low-k dielectric film (k = 2.4) that provides excellent embedding characteristics (see Fig. 10). This low-k film also possesses excellent planarization and thermal resistance up to 800°C, so can be applied to most metallization including tungsten (W) interconnects used as bit-lines and Al interconnects used as PMD (pre-metal dielectric) layers.

CONCLUSIONS

This paper reviewed the current status of research and development in 2007 on ULSI devices, focusing on the technology boosters that have been identified by the ITRS (International Technology Roadmap for Semiconductors). While these technologies are essential to sustain and extend improved transistor performance in the years ahead, most are behind schedule in terms of the original optimistic projections of the ITRS. This underscores the enormous challenges involved in making further headway in transistor performance that does not simply rely on continued

reduction of minimum device dimensions.

Now that further downscaling of device features has become so difficult, this also suggests the need to go beyond the categories identified by the Roadmap and the importance of greater diversity and hybrid technologies where wide ranging devices are monolithically integrated such as the SoC (system-on-chip) approach for future ULSI device development. For example, one area of growing R&D interest and progress is hybrid devices combining non-volatile memory, RF (radio frequency)-based passive elements, and silicon optical elements.

REFERENCES

(1) ITRS, http://www.itrs.net/
(2) D. Hisamoto et al., IEEE Trans. Electron Devices, Vol.38, p.1419 (1990).
(3) D. Hisamoto et al., IEEE Trans. Electron Devices, Vol.47, p.2320 (2000).
(4) F. Yang et al., IEDM Tech. Dig., p.255 (2002).
(5) H. Shang et al., VLSI Symp., p.54 (2006).
(6) H. Kawasaki et al., VLSI Symp., p.70 (2006).
(7) J. Bhavnagarwala et al., IEEE J. Solid-State Circuits, Vol.36, p.658 (2001).
(8) P. A. Stolk et al., IEEE Trans. Electron Devices, Vol.45, p.1960 (1998).
(9) J. Hubbard et al., J. Mat. Res. 11, p.2757 (1996).
(10) W. Peacocket et al., J. Appl. Phys. 92, p.4712 (2002).
(11) T. Kawahara et al., Mat. Res. Soc. Symp. Proc. 745, p.155 (2003).
(12) S. Saito et al., J. Appl. Phys., Vol.98, p.113706 (2005).
(13) K. Torii et al., IEEE Trans. Electron Devices, Vol.53, p.323 (2006).
(14) C. C. Hobbs et al., IEEE Trans. Electron Devices, Vol.51, p.971 (2004).
(15) K. Shiraishi et al., VLSI Symp., p.108 (2004).
(16) Y. Shimamoto et al., VLSI Symp., p.132 (2005).
(17) M. Suzuki et al., IEDM Tech. Dig., p.39 (2005).
(18) T. Hayashi et al., IEDM Tech. Dig., p.247 (2006).
(19) K. Takahashi et al., IEDM Tech. Dig., p.91 (2004).
(20) K. Shiraishi et al., IEDM Tech. Dig., p.445 (2005).
(21) A. Shima et al., VLSI Symp., p.174 (2004).
(22) T. Ito et al., Ext. Abst. of SSDM, p.182 (2001).
(23) D. Jacobson et al., Ext. Abst. of IIT, p.300 (2000).
(24) V. N. Faifer et al., J. Vac. Sci. Technol. B24 (1), p.414 (2006).
(25) C. L. Petersen, et al., Appl. Phys. Lett. 77, p.3782 (2000).
(26) A. Shima et al., J. Appl. Phys., Vol.89, No.6, p.3458 (2001).
(27) P. D. Wolf et al., J. Vac. Sci. Technol. B18 (1), p.540 (2000).
(28) Y. Hayashi, Proc. IITC, p.145 (2002).
(29) D. Edelstein et al., IEDM Tech. Dig., p.773 (1997).
(30) J. Koike et al., Proc. IITC, p.161 (2006).
(31) D. Ryuzaki et al., IEDM Tech. Dig., p.949 (2004).
(32) H. Sakurai, et al., "Interlayer Dielectric Material HSG-255 with Low Dielectric Constant for ULSI," Hitachi Chemical Technical Report, No. 42, p.49 (2004).
(33) T. Furusawa et al., Proc. IITC, p.45 (2005).
(34) K. Kin, IEDM Tech. Dig., p.333 (2005).
(35) D. Ryuzaki et al., VLSI Symp., p.136 (2006).

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