New Model CD-SEM for 45-nm Devices and Beyond

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OVERVIEW: In next-generation optical exposure technology, a liquid immersion technique is employed to enable the use of hyper-NA optical systems in which the lens has an NA of more than 1.0. The use of techniques such as resolution enhancement implementing low-k1, OPC and double patterning has also made it possible to achieve the utmost resolution, but to ensure that patterns are formed stably it is essential to address the issues of reduced focal depth and process tolerance. In measuring techniques, to adapt to these advanced techniques it is necessary to achieve higher measurement accuracy and improved rendering of 3D profiles. The latest CG4000 CD-SEM equipment is a next-generation CD-SEM adapted to these market trends. Furthermore, the DesignGauge design data utilization system supports the improved precision of OPC models required by next-generation exposure techniques, and is compatible with the trend for rapid growth in the number of measurement points.

INTRODUCTION

CD-SEMs (critical dimension scanning electron microscopes) are widely used as the main tool for CD measurement in semiconductor processes. In recent years they have helped in achieving improved precision for smaller design rules, and faster measurements for greater numbers of measurement points. New functions have also been implemented, such as automation of measurements through the effective utilization of design data, and measurement of hazardous locations using positional information.

Liquid immersion exposure is an advanced technique that can implement hyper-NA (numerical aperture) optical systems where the lens has an NA of more than 1.0. It is also possible to achieve the utmost resolution by employing techniques such as resolution enhancement techniques to implement low-$k1$, advanced OPC (optical proximity correction) and double patterning. However, to ensure stable pattern formation, it is essential to address the problems of reduced focal depth and process tolerance. To achieve stable device characteristics, it is also essential to employ 3D (three-dimensional) device structures such as fin-shaped gates, and to form these shapes stably as the aspect ratio of the electrode through-holes increases.

With regard to measurement techniques, progress is being made at improving the implementation of 3D shapes by making further improvements in measurement precision to address the issues of the above-mentioned leading-edge technology.[2]

This article discusses the CG4000 next-generation CD-SEM as a measurement device that can meet the demands of next-generation devices, and the DesignGauge design data utilization system which uses design data to perform measurements (see Fig. 1).

PROBLEMS OF MEASUREMENT TECHNIQUES IN NEXT-GENERATION LITHOGRAPHY

Addressing Problems of Next-generation Lithography

In next-generation exposure techniques, progress is being made in increasing the NA of the lens and reducing the $k1$ value through the use of liquid immersion techniques. Technologies that are being used to implement this include RET (resolution enhancement technology), advanced OPC technology and DP (double patterning) technology (see Fig. 2). Beyond an hp (half pitch) of 45 nm, it is essential to make advances in very difficult techniques such as

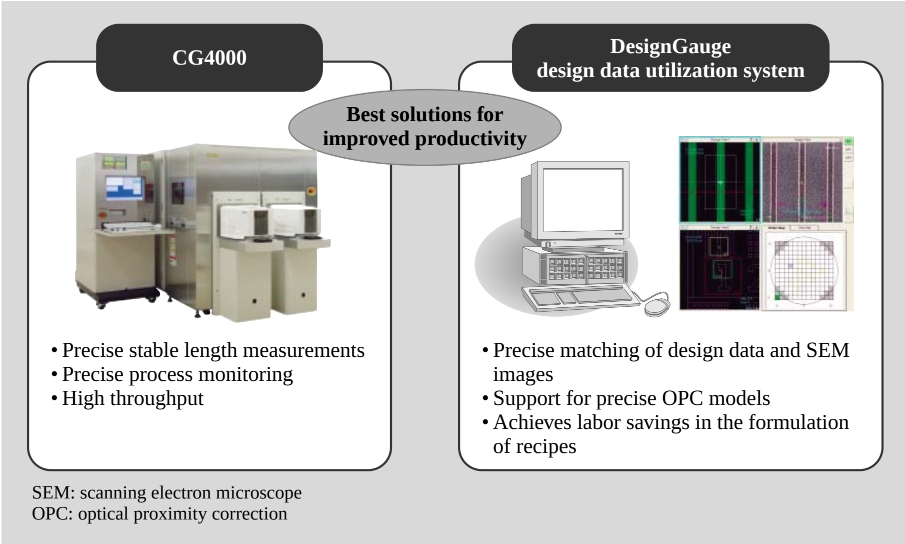

Fig. 1—The New CG4000 CD-SEM (critical dimension scanning electron microscope) System and DesignGauge Design Data Utilization System.
Hitachi High-Technologies Corporation has developed the new CG4000 CD-SEM measurement system, which is adapted to the severe demands of next-generation device fabrication processes, and the DesignGauge design data utilization system which is useful for designing and developing semiconductor devices more efficiently and improving their yield.

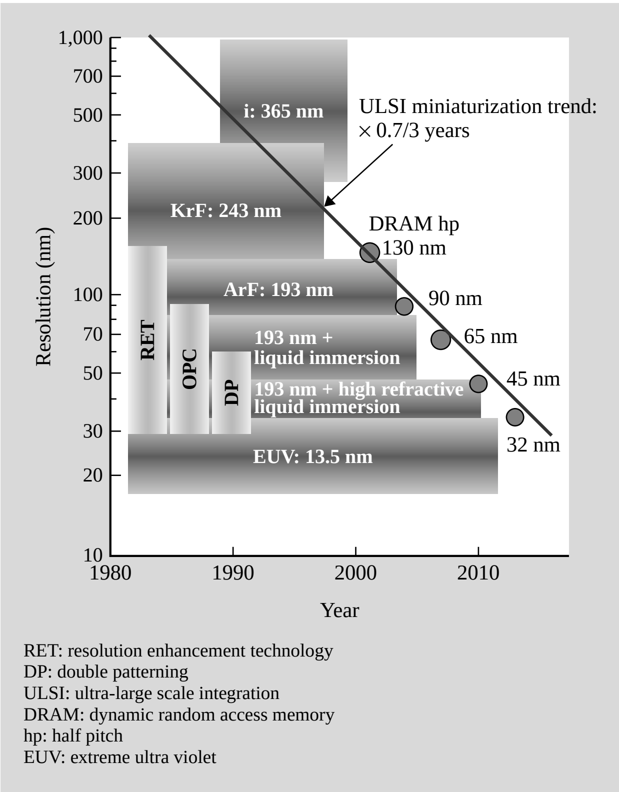

Fig. 2—Recent Trends in Lithography Scale Reduction.
Lithography processes are accelerating towards 45 nm and beyond.

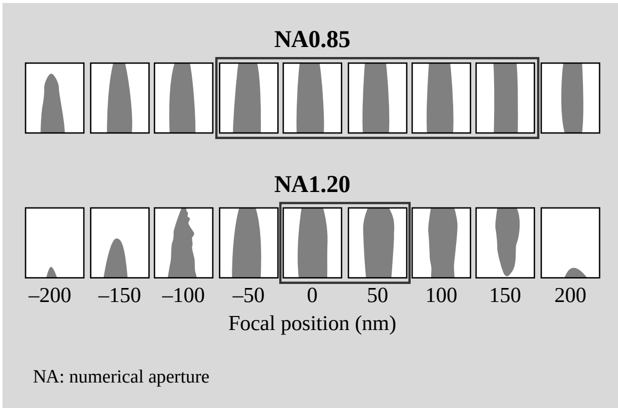

Fig. 3—Simulated Reduction of Focal Depth with Increasing NA (90 nm Isolated Line).
Simulated pattern cross sections obtained when resolving a 90 nm line with ArF liquid immersion exposure at NA 0.85 and NA 1.20.

liquid immersion exposure using materials with high refractive index, and EUV (extreme ultraviolet) exposure at a wavelength of 13 nm. Fig. 3 shows how increasing the NA of a lens results in lower focal depth. This figure also shows the results of simulating pattern cross sections formed when 90-nm lines are resolved by ArF liquid immersion exposure with numerical apertures of 0.85 and 1.20.

At NA=0.85, the pattern is well formed over a wide range of focal positions, whereas at NA=1.20 the range over which the pattern is stably formed is reduced by roughly half. Thus, although increasing the NA allows the resolution limit to be improved, it also results in a significant reduction in focal depth, making it essential to precisely manage the parameters that affect focal depth. Even in CD-SEM measurements, it is important to represent not simply the dimensions at the bottom part of the pattern, but also the three-dimensional profile of the pattern cross section.

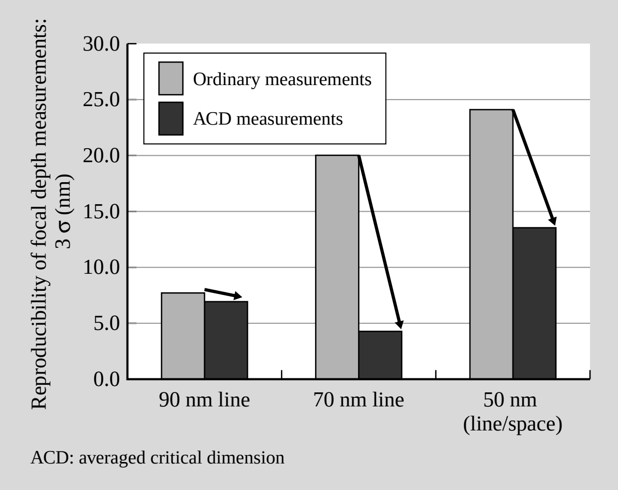

Fig. 4—Examples of PW (process window) High-precision Measurements (Illustrating the Benefits of ACD Measurements).
A comparison of ordinary single-pattern CD measurements and ACD measurements where multiple patterns are measured simultaneously.

Fig. 5—The CG4000 CD-SEM System for the 32-nm Process Node.
An external view of the new CG4000 CD-SEM system is shown.

PW Evaluation

In the implementation of low-*k*1 lithography, it is important to consider countermeasures to the reduction of process tolerances such as DOF (depth of focus) and exposure tolerance. PW (process window) analysis is an important task for expressing these tolerances. PW is widely used not only in the evaluation of basic line/space patterns but also for the evaluation of locations that are unsuitable for OPC and dangerous locations in circuit patterns. It is also widely utilized for purposes such as the optimization of process conditions and process management in manufacturing environments. For these reasons, the precise evaluation of PW is a major issue in measurement techniques.

PW forms a pattern while varying the exposure equipment's focal position and exposure level in a matrix, and determines focal position and exposure level at which the target dimensions are obtained. In this process, the CD of a pattern is obtained by CD-SEM, but the precision of CD measurements must be improved to obtain precise PW measurements. One example of how PW measurements can be made more accurate is illustrated in Fig. 4[2], which compares the results obtained using ordinary single-pattern CD measurements with ACD (averaged CD) measurements made simultaneously from multiple patterns. Three types of pattern are compared here, and in each case it can be seen that the measurement reproduction accuracy is improved. In particular, this improvement effect becomes larger as the pattern becomes narrower. Thus as lithography processes move towards narrower patterns, the shapes of patterns formed by these processes vary more widely leading to reduced measurement accuracy. In CD measurements, it is essential to have a firm grasp of these variations, and to develop measurement applications that take these variations into account.

CG4000: CD-SEM FOR 32-NM PROCESS NODE

The New CG4000 Next-generation CD-SEM

The expectations and demands being placed on measurements by CD-SEM in next-generation lithography are continuing to grow. As the manufacturer of the CD-SEM equipment with the largest share of the global market (according to a 2005 survey by Gartner Dataquest) Hitachi High-Technologies Corporation has developed the new CG4000 CD-SEM which responds to the demands of the market and leads the market needs, and has begun to make this system commercially available (see Fig. 5). The main features of the CG4000 are discussed below.

For a next-generation CD-SEM that can adapt to process development beyond 32 nm and mass production at the 45-nm process node, functions for the application of technologies such as OPC, liquid immersion exposure and double patterning are of course a necessity. However, it is difficult to fully address the problems with application functions alone,

Table 1. Measurement Reproducibility Requirements of CD-SEM
CD-SEM is required to achieve a very high level of measurement reproducibility at the sub-nanometer level.

Year	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016
DRAM 1/2 pitch (nm)	80	70	65	57	50	45	40	36	32	28	25	22
MPU gate length (physical) (nm)	32	28	25	22	20	18	16	14	13	11	10	9
Required precision of dimensional measurements (nm) Isolated line 3 σ	0.67	0.58	0.52	0.46	0.42	0.37	0.33	0.29	0.27	0.23	0.21	0.19
Required precision of dimensional measurements (nm) Packed lines 3 σ	1.77	1.49	1.33	1.18	1.05	0.94	0.84	0.74	0.66	0.59	0.53	0.47
Required precision of dimensional measurements (nm) Contact hole 3 σ	2.08	1.76	1.57	1.40	1.25	1.10	0.98	0.88	0.78	0.69	0.61	0.56

Countermeasures available　Production countermeasures available　No countermeasures

Source: ITRS (International Technology Roadmap for Semiconductors) (2005)

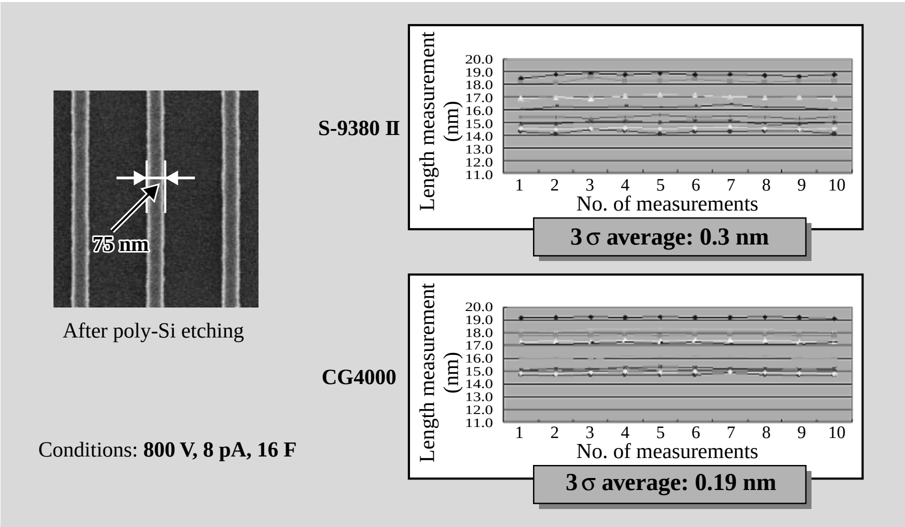

Fig. 6— Dynamic Reproducibility. In the CG4000, the precision of pattern dimension measurements is increased to achieve superior dynamic reproducibility.

and it is important to develop a solution that combines precise high-stability length measurements and application functions. The CG4000 is a CD-SEM that enables anyone to perform precise stable length measurements in processes with a hp of 45 nm or beyond.

To realize this aim, Hitachi made a comprehensive review of conventional systems, allowing them to realize precise stable length measurement.

Precise Length Measurement Capability

The expectations and demands placed on CD-SEM measurements in next-generation processes are continuing to grow. Variation in pattern dimensions has a large effect on device characteristics, so for example in a 65 nm MPU (micro processing unit) device with a gate width of 25 nm, the CD control must be performed with a very high accuracy of 2.6 nm (3 σ). The required value for measurement reproducibility in CD-SEM is also required to have a very high value at the sub-nanometer level as shown in the ITRS (International Technology Roadmap for Semiconductors) (see Table 1). To achieve this high measurement reproduction accuracy, it is necessary to develop measurement techniques that take into consideration the avoidance of electrostatic phenomena that affect the measurement precision, and the use of new materials, processes and structures such as SOI (silicon on insulator) and low-*k*1 films.

The CG4000 increases the pattern dimension measurement accuracy to achieve a maximum resolution of 1.8 nm at 800 V, and a dynamic reproducibility in wafer loading and unloading of 0.3 nm (3 σ, using standard Hitachi wafers) (see Fig. 6).

The measurement accuracy of the CG4000 can resolve the so-called "red brick wall" (lack of solutions to technical problems) that the ITRS predicts will occur after 2010, and has thus enabled further progress to be made in the miniaturization of semiconductor devices.

To achieve improvements in the basic performance, a wide variety of technologies are driven in order to acquire SEM images more stably in addition to the electro-optical system technology that is the core competence of Hitachi. This has allowed further improvements to be made to the resolution and measurement reproducibility. On top of the basic performance achieved in this way, Hitachi has placed measurement technology that is compatible with a wide range of new materials and new processes in semiconductor devices, and application technology that responds to the users' needs. Some of the newly developed measurement technologies are discussed below.

Dealing with Charge Build-up in Wafer

The build-up of electrostatic charge in the wafer is a major factor behind the reduction of measurement reproducibility. In measurements of non-conducting materials, electrostatic charge builds up inside the wafer, causing it to repel the electron beam and cause focusing errors. Focusing errors occur when there are different amount of charge in different parts of the wafer, resulting in reduced measurement precision. In extreme cases, measurement errors may occur, making automatic measurement impossible. This phenomenon varies widely between different materials and processes, so it is necessary to develop techniques to cope with each situation.

In developing the CG4000, Hitachi researched these electrostatic phenomena and studied how to deal with them. These phenomena can be broadly divided into cases where the electrostatic charge is distributed with and without axial symmetry relative to the center of the wafer. The CG4000 incorporates functions for dealing with both types of electrostatic phenomena. When the charge is distributed with axial symmetry, the electrostatic charge is measured with a voltmeter and the measurement accuracy is improved by employing a technique whereby the charging is compensated by using approximation curves. In the case of asymmetrical charging, compensation has to be performed at each measurement site, and the equipment includes a new autofocus system for this purpose. In addition, non-point situations can also occur, in which case measurements cannot be made, but by incorporating new non-point compensation technology the equipment is able to deal comprehensively with electrostatic phenomena.

Process Monitoring

As semiconductor devices become more miniaturized and processes become more complex, the need arises to cope with production management issues from various different viewpoints.

In the production of DRAM (dynamic random access memory) and system LSI (large-scale integration), it is very important to improve product yields. The key to achieving and maintaining high yields is to somehow implement precise and rapid monitoring and feedback of process fluctuations. From these needs for high reproducibility and high speed, The introduction of scatterometry/OCD (optical CD) measuring equipment as tools for process monitoring is widely investigated in lithography and etching processes . In scatterometry methods, the pattern shape is estimated by matching the intensity of light reflected from the actual pattern to a library of results obtained in wave optics simulations of the wavelength dependency (or incident angle dependency) of the reflected light intensity obtained with a model pattern. The measurements are performed using a special pattern with a grating (line and space) structure spread over a 50 μm × 50 μm area. This approach is characterized by the ability to obtain averaged pattern dimensions while avoiding the effects of roughness and the like. Drawbacks of this approach include the fact that experience is needed to compile such a library, so that a long time is required to formulate recipes, and the fact that it is difficult to measure real patterns in devices.

For CD-SEM, Hitachi is developing a variety of application technologies to deal with high-speed measurements and averaged measurements, and obtaining values that rival the results obtained by scatterometry.

The CG4000 incorporates an ACD functions including averaged measurement functions and multi-pixel image acquisition functions with an increased number of pixels for SEM images. This makes it possible to obtain measurement precision at least as good as that of length measurements with a large scale factor by employing averaged measurements with a low scale factor (see Fig. 7).

The CG4000's ACD functions employing multi-pixel images can be used to measure not just repeating

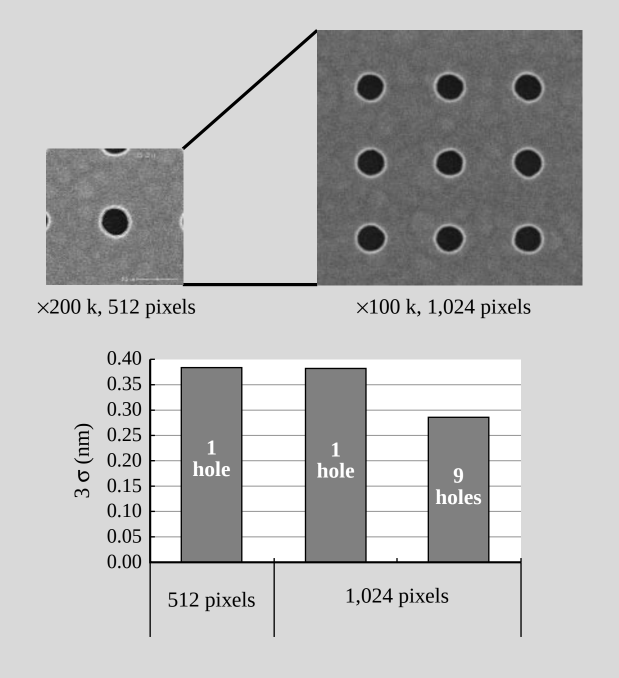

Fig. 7—Example of Hole Measurements by Multi-pixel ACD.
The combination of multi-pixel images and ACD allows averaged measurements to be made at low scale factors with the same precision as length measurements at high scale factors.

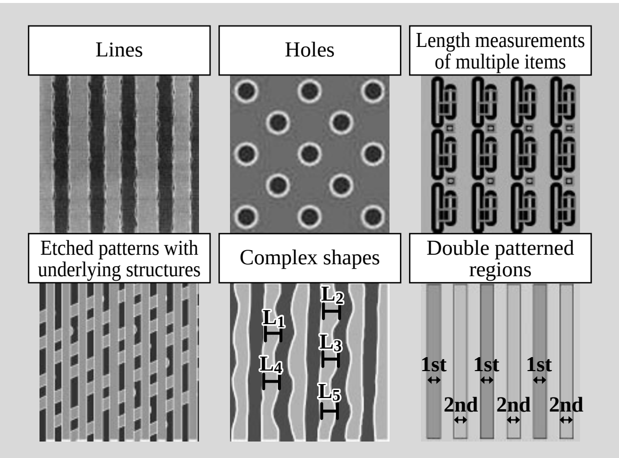

Fig. 8—Process Monitoring of Diverse Profiles by Multi-pixel ACD.
Multi-pixel ACD can be used to measure a wide variety of patterns including etched patterns.

patterns but a wide range of patterns that have caused problems with OCD, including etched patterns with underlying structures. This makes it possible to perform stable process monitoring more reliably (see Fig. 8).

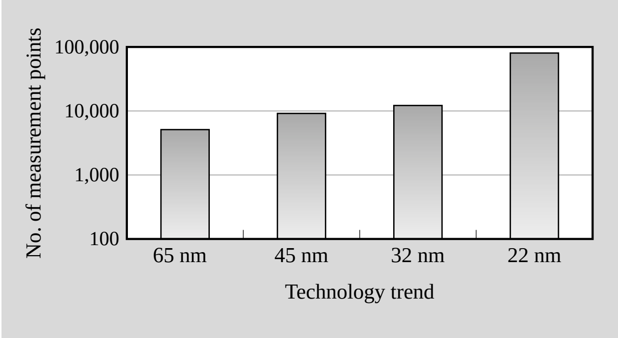

Fig. 9—Increasing Numbers of Measurement Points due to Miniaturization.
The number of CD measurement points continues to grow.

Increasing the Number of Measurement Points

As semiconductor devices become more miniaturized, major technical issues arise such as the increasing complexity of OPC and the increased effects of mask errors. From these circumstances, attempts to increase the device yield are liable to cause lithography defects. It is important to find dangerous locations (hot spots) and to take measures to reduce problems in these parts. Alternatively, measures will have to be taken such as DFM (design for manufacturability) where measures are taken by incrementally modifying the design.

The number of CD measurement points used in creating OPC models and verifying the performance of OPC is steadily increasing, and run into the thousands or even tens of thousands (see Fig. 9). It is predicted that hot spot management will eventually become necessary on production lines. To cope with this increasing number of measurement points, it is not sufficient merely to increase the throughput of devices—achieving reductions in the time and effort needed to create measurement recipes is also an important issue.

To implement accurate measurements of pattern dimensions with CD-SEM, the field of view of the SEM image has to be aligned to an arbitrary measurement location in the wafer within an error of no more than a few tens of nanometers. Actual measurements consist of a sequence of actions including stage movement, addressing, image acquisition and pattern measurement, which are performed in a unit called a measurement recipe. Once a measurement recipe has been created, it can be used by an operator or the like to perform measurements automatically (see Fig. 10).

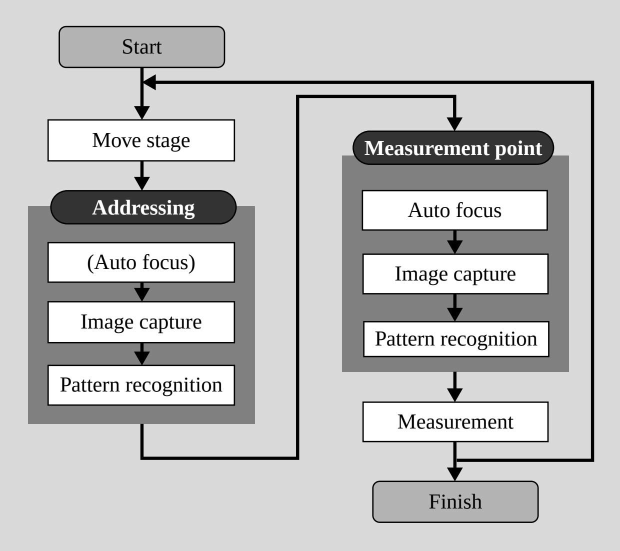

Fig. 10—Example of a CD-SEM Measurement Recipe.
Once a measurement recipe has been prepared, measurements can be made automatically without the operator's involvement.

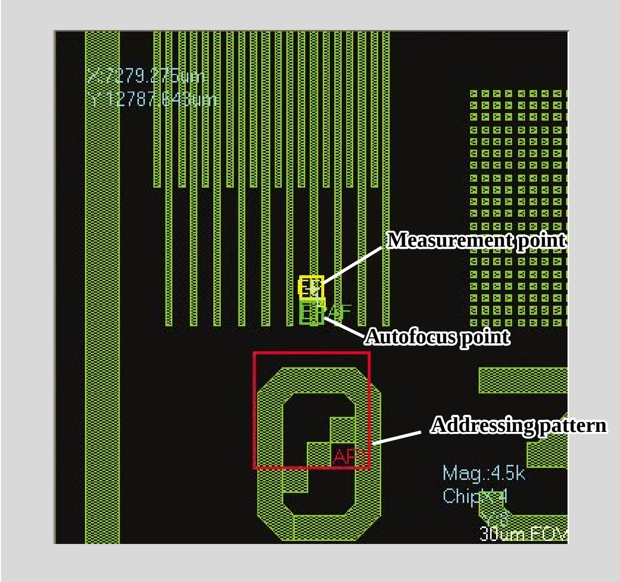

Fig. 11—Specifying Measurement Points in the Design Data.
Allows templates to be registered more easily and facilitates the rapid preparation of measurement recipes.

The detection of measurement patterns in CD-SEM measurement recipes is performed using pattern recognition based on image processing technology. An SEM image of an actual pattern is used as a template for this purpose. The registration of templates is performed manually by the operator producing the measurement recipe. When there are multiple locations to measure, an SEM image template must be registered for each measurement point, and this operation can take a long time when creating actual recipes. As a result, engineers have to devote a lot of their time to the preparation of measurement recipes, which is a major problem. In the latest CD-SEM, this problem is also addressed.

Measurements at Multiple Points with DesignGauge

To address the issues of next-generation processes, Hitachi developed a design data utilization system called DesignGauge to facilitate observations and measurements in which top-down observation images are contrasted against the design data.(3) DesignGauge not only connects to S-9380II 65-nm generation equipment, but can also connect to the CG4000.

Hitachi developed functions for increasing the efficiency of creating measurement recipes for large numbers of measurement points. Compared with conventional methods that use actual SEM images, the creation of measurement recipes from design data has the following two benefits:(4)

(1) No need for CD-SEM or wafers

Hitherto, addressing has entailed creating an SEM image template using an actual wafer. In Hitachi's new method for creating templates based on the design data, there is no need for a wafer to take measurements from, allowing recipes to be created in advance so that the measurement recipe can be put into action as soon as the wafer has been created.

(2) Creation of multiple point measurement recipes

The measurement point coordinates and addressing point coordinates are all written to a measurement point data file (HSS file), and are transformed into a measurement recipe all at the same time, so that a measurement recipe can be produced in a short time even when there are thousands of measurement points. Also, since an addressing template can be automatically produced from the design data, it is possible to simplify the registration of templates which has taken up the most time and effort in the preparation of measurement recipes for CD-SEM (see Fig. 11).

Thus by employing DesignGauge, it is possible to produce measurement recipes easily.

With this function, the time taken to create measurement recipes can be reduced to about one tenth of the time needed in conventional CD-SEM when there are a few thousand or so measurement points

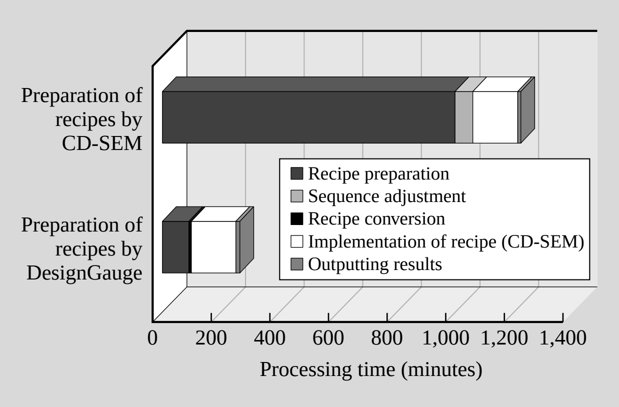

Fig. 12—Comparison pf Processing Time.
The results of using DesignGauge to prepare measurement recipes.

(see Fig. 12). Thus in the future it will be possible to perform multiple point measurements in a short time using CD-SEM, which can make a great contribution to improving the yield of wafers at the cutting edge of technology.

CONCLUSIONS

This article has discussed the new CG4000 CD-SEM system which is adapted to mass production at a half pitch of 45 nm and subsequent process development, and the DesignGauge system for the utilization of design data to resolve the issues of next-generation measurement techniques.

As the patterning techniques used for semiconductor devices continue to challenge the limits of resolution, Hitachi High-Technologies Corporation is supporting the development of devices by providing measurement technology. In particular, in the measurement techniques of the future, the accuracy of measurements will be called into question, especially the precision of length measurements. It is thought that this trend will become even more important in the future. Hitachi intends to further develop its core competence of electron beam applications, and to contribute to the measurement aspects of device technology.

Also, the recent trend towards DFM is resulting in device designs that are more friendly through the application of manufacturing technology, and thus Hitachi is making an active contribution with regard to the monitoring and quantification of manufacturing process technology.

REFERENCES

(1) S. Owa et al., "Immersion Lithography — Its Potential Performance and Issues," Proc. SPIE Vol. 5040, p. 724 (2003).
(2) T. Ishimoto et al., "Advanced Process Control for Hyper-NA Lithography Based on CD-SEM Measurement," SPIE, 6518-93 (2007).
(3) H. Morokuma et al., "A New Matching Engine between Design Layout and SEM Image of Semiconductor Device," Proc. SPIE Vol. 5752, p. 546 (2005).
(4) H. Sakai et al., "Reticle Pattern Evaluation Technology Using DesignGauge," Proc. SEMI Technology Symposium, p. 2-54-64 (2006).

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