Advanced Defect Review System for Yield Enhancement (RS Series)

Seiji Isogai Fumiaki Endo Kenji Kobayashi Koji Arai OVERVIEW: Recently, in the semiconductor industry, supplying the advanced devices to the market faster than one's competitors at a competitive price has become a key factor determining the success or failure of businesses. Consequently, semiconductor manufacturing processes are accelerating towards reduced feature size and increased complexity, the number of defects that need to be detected is increasing, and inspection equipment is becoming more sensitive. With conventional inspection and analysis procedures, it is becoming increasingly difficult to achieve a fast ramp-up in the yield of mass production processes. Hitachi High-Technologies Corporation has developed a Defect Review SEM and Application systems, and has proposed solutions for the efficient extraction of useful data for process improvement and process control from the large volume of defects in semiconductor manufacturing processes.

INTRODUCTION

IN the manufacture of semiconductor devices with a more reduced feature size, greater sensitivity is needed

for the inspection of these devices and the number of defects need to be detected becomes very large. A particularly important issue is how to quickly extract

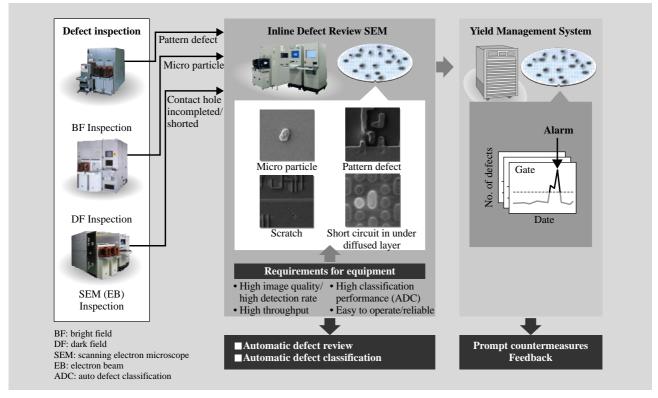


Fig. 1—Hitachi's Defect Review System Concept.

Hitachi's Defect Review SEM provides a fast and accurate tool for automatically observing defects and the automatic classification of these defects detected by wafer inspection equipment. The classification data is managed on the yield management system, and is also used to extract the source of problems so that quick feedbacks can be applied to the process as soon as possible.

information that is useful for process control and yield management. Also, since new materials are starting to be used in full-scale mass production, such as low-*k* (low permittivity) materials, SOI (silicon on insulator) wafers and ArF resist materials, it is important to be capable of stable observation and analysis of these diverse materials. Furthermore, immersion lithography technology is being employed for the 65-nm logic process node [i.e. semiconductor fabrication with an hp (half pitch) of 65 nm], and immersion double patterning technology is regarded promising for the hp 45-nm logic process node. As advances are made in this ultra-high resolution technology, the management of systematic defects at critical locations (hot spots) is also regarded very important.

The problems of low yield associated with reduced feature size and the introduction of new materials and more complex processes need to be addressed quickly in order to achieve a fast ramp-up. In the future it will be necessary to review and classify defects automatically to implement systems that extract large amounts of information from defects and efficiently analyze this information immediately after defects have occurred in production processes so that it can be promptly fed back to the manufacturing equipment, manufacturing conditions, and process integration.

This article discusses a defect review system proposed by Hitachi High-Technologies Corporation to implement fast ramp-up in the yield and quality of semiconductor devices (see Figs. 1 and 2).

THE NEEDS OF DEFECT REVIEW SYSTEMS

A defect review system is a system that reviews and classifies defects based on the defect positions

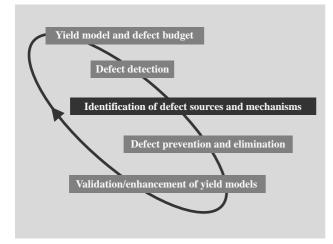


Fig. 2—Yield Improvement Model. The key to improving yield is time to clarify the origins of defects and the mechanism.

output from an inspection equipment, analyzes the defects on all production wafers, and extracts information leading to yield enhancement.

To achieve this, the system must have the following five features:

(1) High resolution to detect small defects

(2) Charge control for stable image quality from any material

(3) High throughput to observe a large number of defects

(4) High-performance image processing for captured defect

(5) Automatic defect classification capabilities with high accuracy

It is also important to acquire diverse information to identify the source of defects. In addition, as recent increases in the complexity of lithography processes are leading to an increased generation of hot spots, it is important to automate tasks that were hitherto performed by manual, such as obtaining images from fixed spot and judging whether or not patterns are formed properly.

The role of a defect review system is to efficiently extract those information and help process engineers make rapid and appropriate decision.

NEW TECHNOLOGIES AND FUNCTIONS SATISFYING THESE NEEDS

New Electro-optical System

In Hitachi's Defect Review SEM (scanning electron microscope), three types of information are extracted from each detected defect: (1) secondary electron image, (2) oblique contrast image by reflected electron, and (3) voltage contrast image (see Fig. 3).

In the image quality obtained by the Defect Review SEM, not only is high resolution important, but it is also important to have information about the oblique contrast of the defect. Hitachi's review SEM achieves high resolution by improving the SN (signal-to-noise) ratio of the SE image (secondary electron image), and achieves improved contrast in the oblique contrast image [UL (upper left)/LR (lower right) image].

Of the electrons originating from the wafer, reflected electrons containing the surface texture information (especially high-energy reflected electrons) are selectively captured and guided to detectors on the upper left and lower right sides by precisely discriminating between the electrons depending on the reflected angles, thereby allowing the oblique contrast to be improved. Also, the highenergy nature of these electrons means that they are

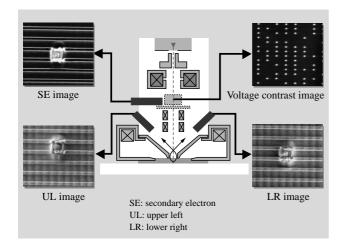


Fig. 3—Simultaneous Acquisition of Multiple Images. Secondary electron images, reflected electron images and voltage contrast images are acquired simultaneously from individual defects.

more immune to charging influences.

High Speed/High Capture Rate ADR and High Precision ADC

To provide useful information for process control and yield management, it is important to accurately acquire large numbers of defect images, classify these images accurately based on their characteristics, and output real-time information on the occurrence of defects that have a high impact on the device yield.

For equipment to realize this, it must have (1) a high throughput, (2) ADR (automatic defect review) with a high defect capture rate, and (3) ADC (automatic defect classification) with a high accuracy. In ADR, Hitachi has achieved both a high capture rate and high throughput by adding an extended referenceless mode in which defects are detected while automatically switching between die comparison modes for peripheral circuit regions and a cell comparison mode for periodical pattern regions. Hitachi also incorporated a multi-pixel imaging mode for the detection of smaller defects.

ADC combines two classification algorithms based on preset rules and based on characteristic quantities of images obtained by using defect images as teaching data. This makes it possible to flexibly select the modes according to classification needs, and realizes a high level of classification accuracy.

Systematic Defect Review (SDM)

With reduced feature size, systematic defects constitute a growing proportion of the defects that lead

to poor yield. Also, as the number of hot spots to be managed increases, it becomes more important to employ SDM (systematic defect monitoring) function that observes the fixed points automatically by Review SEM.

By registering the coordinate data of hot spots to be managed, it is possible to automatically acquire images at identical positions from each die on a wafer, and to monitor them for pattern fluctuations.

APPLICATION EXAMPLES

Improved Shadow Images and Robustness against Charging

An example of the improved shadow image is shown in Fig. 4 (a). It shows a defect (scratch) in a Cu interconnect line, but with better contrast than can be achieved with conventional equipment. This improved contrast allows high accuracy of ADR and ADC.

Fig. 4 (b) shows an example of enhancement of charge-up control. This sample shows a structure after ArF resist development. With conventional equipment, contrast errors are caused by charge-up effects at a beam current of 50 pA, but new equipment allows good images even at 150 pA. With this improved charge-up control, the equipment also facilitates ADR for resist patterns.

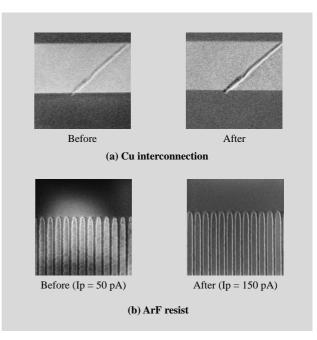


Fig. 4—Improvement of Shadow Images and Robustness against Charging.

Shadow contrast and robustness against charging are improved, and the ADR (automatic defect review)/ADC performance is greatly enhanced.

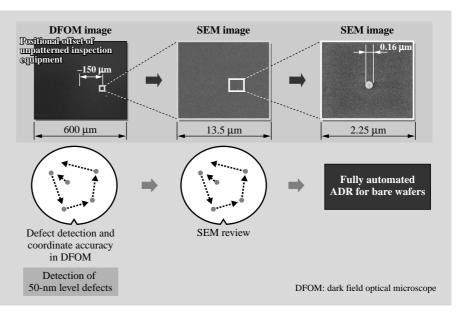


Fig. 5—Bare Wafer Mode ADR Concept. Defects are illuminated by a laser light source and detected by DFOM so that their positions are accurately determined.

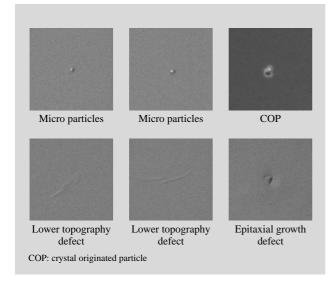


Fig. 6—Examples of Defects Found on Bare Wafers. It has become possible to detect defects that were previously difficult to find with ADR.

Bare Wafer Applications

The concept of bare wafer mode ADR is illustrated in Fig. 5. In general, unpatterned wafer inspection equipment is highly sensitive but has a large fluctuation of coordinates. To deal with this, Hitachi's equipment is fitted with a DFOM (dark field optical microscope) and a laser light source to illuminate defects, determine their positions, and obtain low magnification SEM images from the regions surrounding these defect positions. When defects have been detected in these images, additional high magnification SEM images are obtained centered on these defect positions, allowing SEM images of the defects to be obtained easily.

Fig. 6 shows examples of micro defects detected on a bare wafer. Hitachi's equipment can detect not only micro particle but also other forms of defect such as COP (crystal originated particle) and low contrast defects, and epitaxial growth defects. The equipment can therefore cope with defects and particles of smaller size that need to be managed as devices further shrink in the future.

Example of Application of SDM Functions

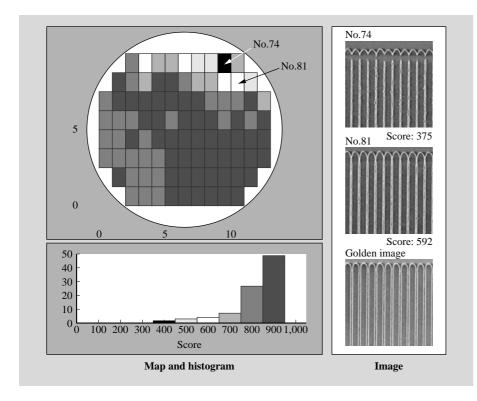
An example of the application of SDM functions is shown in Fig. 7. This figure shows a sample of FEM (focus exposure matrix) ArF resist. From each image and score value, it can be seen that there is a good correlation between goodness of patterns and the scores.

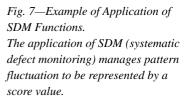
In this way, the acquisition and analysis of large amounts of data (which used to take several days) can be completed in just a few hours. This results in a significant improvement in the productivity.

CONCLUSIONS

This article has discussed the Hitachi High-Technologies Corporation defect review system.

As the lifetime of semiconductor devices decreases, it is becoming essential to reduce the time taken to develop new products and improve their production yield. For this purpose, it is becoming more and more important to employ defect review SEM in the role of





extracting the factors that cause defects to occur. Also, in processes beyond hp 65 nm, there is an increased need for monitoring systematic defects, such as lithography hot spots, and defect review SEM is also expected to be very useful for this purpose.

Hitachi intends to continue marketing activities, strive further for the development and consolidation of applications so we can respond promptly to the users' needs, thereby proposing equipment that is more attractive.

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