Plasma Etching System and its Applications to 45–32-nm Leading-edge Devices

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OVERVIEW: Maintaining the process accuracy of leading-edge semiconductor devices has recently become quite difficult. Dry etching, in particular, is facing many new challenges, such as the application of immersion lithography photo resists, dual metal materials, low-k and high-k materials, in addition to the basic requirements of cost and performance. Hitachi has developed excellent dry-etching equipment and application processes for manufacturing complicated devices that are based on a simplified chamber structure. These processes achieved the targets of 45–32-nm nodes while simultaneously accomplishing high throughput, high yield, and high productivity. A critical dimension uniformity of 1.8 nm, a line width roughness of 3.2 nm, and an isolation-dense bias of 1.0 nm have been achieved for gate etching. Etching rates of 300 nm/min, critical dimension shifts of <5.0 nm, and critical dimension uniformity of 3 nm have been attained for multilayer masks. Time-dependent changes could be reduced to 1.2% using process-control technology. Hitachi has already confirmed these features in 45-nm-node pre-manufacturing.

INTRODUCTION

45-nm-NODE semiconductor devices are being produced worldwide and 32-nm-node processes are being developed. Hitachi has developed excellent dry-etching equipment and processes that can achieve high throughput, high yield, and high productivity in the manufacture of these complex devices.

Dry etching is a chemical reaction between semiconductor-wafer surface materials and reactive gases within the plasma. Photo-resist materials create patterns on semiconductor wafers during the lithography process and serve to protect areas where reactions are not required. The lithography process actually creates feature sizes (patterns) that are smaller than the exposure wavelength (193 nm for ArF excimer exposure) used to create these patterns for leading-edge semiconductor devices. Therefore, many technologies to enhance resolution have been widely applied that often have an adverse impact on dry etching. Dry-etching technologies must not only overcome the negative impact on enhancing resolution, but also improve patterning accuracy.

New concerns regarding yield-related issues are already being seen in addition to typical concerns regarding manufacturing variations in 45–32-nm nodes. The reason is that even very small variations from the CD (critical dimension) or taper angle within a 300-mm wafer may have a large impact on final yields. This situation is conspicuous in 65-nm nodes or less and thus strict targets for uniformity are required by the end users of equipment. Improvements to productivity on the other hand, that have driven down wafer costs are also serious issues. Fig. 1 outlines tactics used for increasing productivity. Equipment productivity clearly plays a major role in decreasing costs. However, the major index, OEE

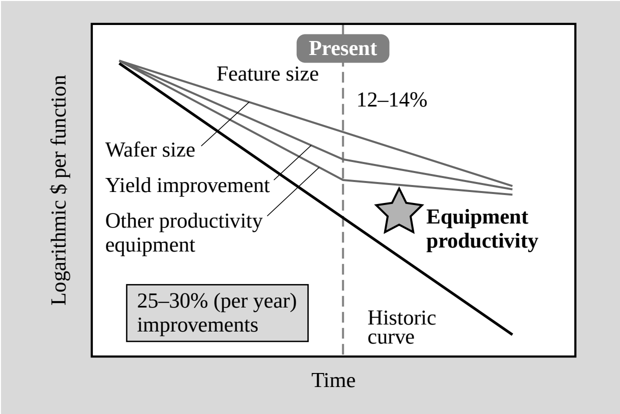

Fig. 1—Tactics for Improving Productivity.
The chip functional cost should be reduced by 25 to 30% per year by reducing feature size, improving yield, and increasing productivity. The measures for improving productivity are the most important.

(overall equipment effectiveness), of equipment productivity is still lower than 50%. The main reasons for low OEE are QC (quality control) operations using the NPW (non-product wafer), scheduled down time, and unscheduled down time. As these are common conditions throughout the world, the ITRS (International Technology Roadmap for Semiconductors) is discussing methods of increasing OEE. ITRS listed six major items [1],[2]

(1) Resource-consumption management
(2) Time-dependent performance changes and compensation
(3) Machine-to-machine differences and adjustments
(4) NPW management and control
(5) Chamber wet cleaning and specifications
(6) Equipment maintenance and rules

These issues are being studied globally and almost all solutions have now been standardized. Hitachi, as an equipment vendor of a critical process tools, is designing technologies that will conform to ITRS requirements, i.e., it is applying stabilizing measures to decrease machine-to-machine variation and time-dependent changes. The details are described below.

DESIGN OF HITACHI EQUIPMENT

SIMPLIFIED ETCHING REACTIONS

The relationship between process settings and process results is plotted in Fig. 2. Process results are not generally directly controlled by process settings because the wafer itself is exposed in a reaction environment that is subjected to many disturbing factors. These influences are much more serious in leading-edge manufacturing. Therefore, measures for stabilization cannot be introduced without reducing the influence of disturbing factors.

Several countermeasures have been investigated to reduce the complexity of present etching process. We need to:

(1) Establish a simple etching model through improving hardware,
(2) Set up independent tuning knobs to adjust etching and install sensors to monitor this,[5]
(3) Position the knobs and optimize the process based on the simplified etching model, and
(4) Construct AEC (advanced equipment control)/APC (advanced process control) systems based on the simplified model, installed sensors, and tuning knobs.[6]

Above all, the most important matters are to establish a simplified model and control it based on the established model. Simplification can be

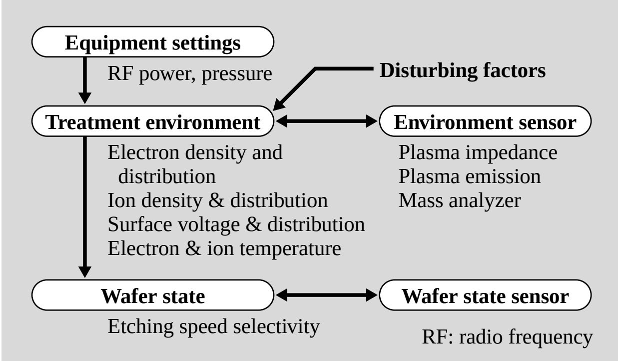

Fig. 2—Relationship Between Equipment Settings and Wafer State.
Wafer states are not directly related to equipment settings in the process equipment. There are treatment environments between the equipment settings and wafer states, and they are susceptible to many disturbing factors.

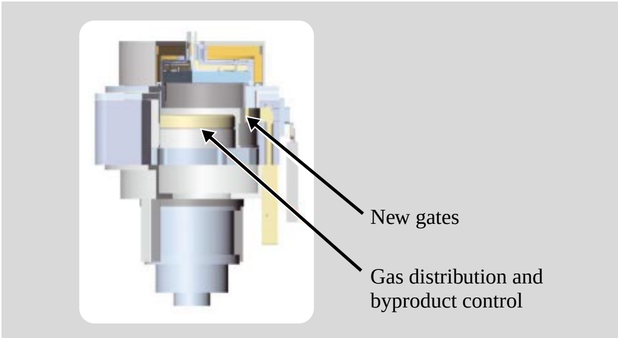

Fig. 3—Completely Symmetrical Chamber Structure.
A completely symmetrical layout for all functional parts achieved a simple distribution for efficient etching. Etch uniformity can easily be modified by adjusting a few tuning knobs.

accomplished by applying coaxially installed turbo molecular pumps, symmetrically designed electrodes, and specially designed variable conductance valves to a completely symmetrical reaction chamber, as shown in Fig. 3. Etching can be improved to have the required symmetrical distribution using this design.

High-volume exhaust systems and low-pressure reactions, which are possible using a high-frequency discharge mechanism with electromagnetic coils, will be used to reduce the influence of disturbing factors in the next step.

Appropriate tuning knobs with features below were introduced to this new concept for dry-etching equipment.

(1) Source power and coil current for incident ion distribution
(2) A two-directional and concentration-controlled gas flow system for radical distribution
(3) Control of the slope of wafer temperature for the

absorption distribution of reaction byproducts

Approaches to stabilizing equipment are often different for users, and thus hardware, processes, and software solutions need to be well balanced.

Two functions are necessary to maintain the stability of equipment and processes. We need to:

(1) Verify the proper functionality of all equipment actuators through feedback, and

(2) Monitor and control the process stability of all chambers based on the reaction model.

Function (1) is easily achieved because root-cause problems are directly indicated by errors. Function (2) is difficult to directly identify, on the other hand, because errors originate from complex root causes and disturbance factors. Therefore, new processes such as AEC and APC gradually become more effective through development from the design of basic to more complex equipment.

GATE PROCESS APPLICATIONS

Gate processes pose numerous challenges in beyond 45-nm-node devices, e.g., in metal gate materials, high-*k* dielectric materials, immersion photo resists, and drastic reductions in CDU (critical dimension uniformity). These are the next device requirements.

Pattern Sidewall Smoothing

Photo-resist patterns in present immersion-type lithography have greater roughness characteristics than those permitted by device requirements. This roughness is called LWR (line width roughness). LWR should be reduced to values of 4 nm or less in dry-etching processes. Hitachi has developed several methods of reducing LWR, as outlined in Fig. 4. The vertical line indicates the degree of LWR and the horizontal line shows the CD shift from the original. The results for the coating 1 method were based on trimming after fluorocarbon was deposited and those for coating 2 were based on trimming after bromine-containing materials were deposited. These two methods were selected from CD requirements and achieved 3.2-nm LWR. A new curing process was also developed without trimming for zero CD shift. Fig. 5 shows the excellent results obtained with the new curing process.

Excellent CD Uniformity and Low Isolation-dense Bias

High-yield manufacturing not only requires high CDU, but also less bias between isolation and dense patterns within 300-mm-diameter wafers. The independent tuning knobs on Hitachi's dry etching equipment can control the reaction position-by-position and can easily achieve excellent CDU. ECR (electron cyclotron resonance) technology can control

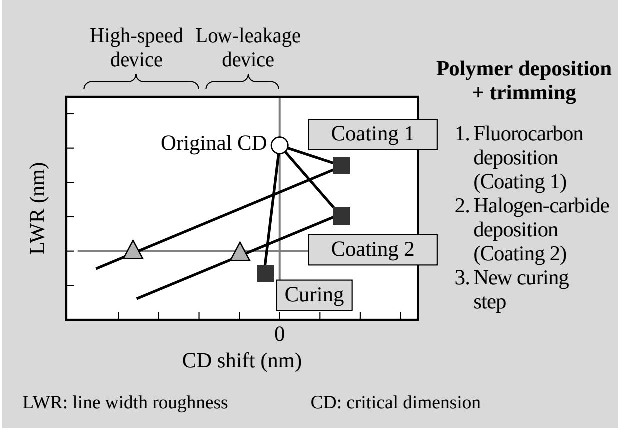

Fig. 4—Methods of Reducing LWR by Dry Etching.
Three methods of reducing LWR are developed. Instead of conventional polymer deposition and trimming, a new curing method without CD shift is newly developed.

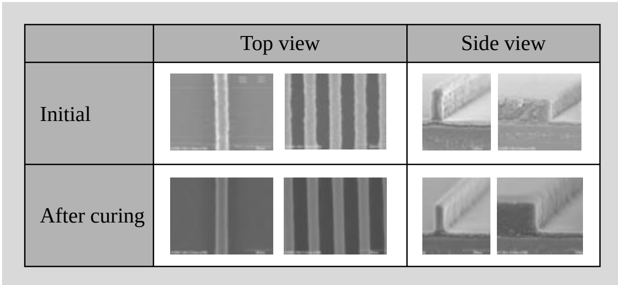

Fig. 5—Effects of Plasma Curing.
The new curing step with a plasma process achieved a smooth side-wall for photo-resist patterns and a low LWR without CD shift.

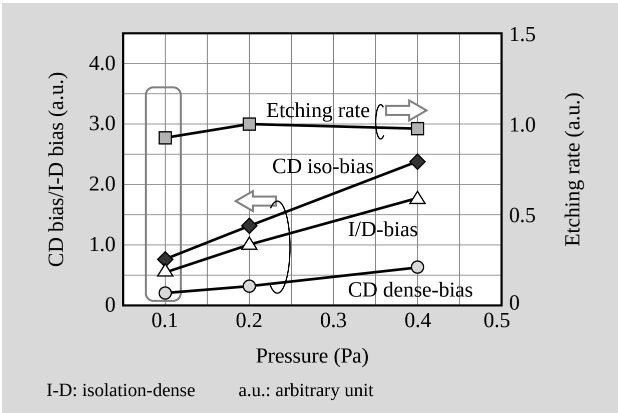

Fig. 6—Relationship Between CD/I-D Bias and Process Pressure.
All CD biases can be reduced by a low pressure reaction. Hitachi can maintain a high etch rate in the low pressure region by using a distinctive plasma source.

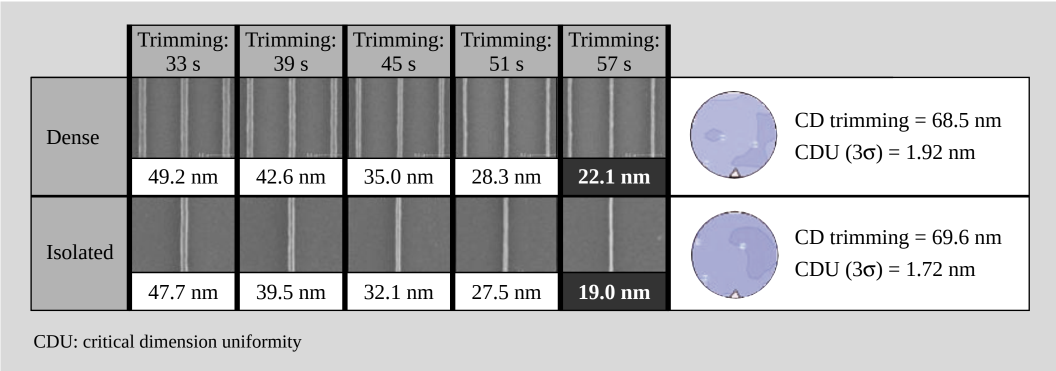

Fig. 7—Trimming Results with No Damage to Photo Resist.
Liner trimming without any wiggling or line breaking were achieved. Small CD patterns of less than 20 nm with excellent CD uniformity can easily be obtained.

ions and radicals independently for low isolation-dense bias and can work well in very low-pressure regions where the ion path is quite straight. The CD shift/I-D (isolation-dense) bias dependence on pressure is plotted in Fig. 6. CDU values of 1.8 nm and I-D bias values of 1.0 nm were achieved by using these low-pressure conditions. Hitachi intends to develop the further low-pressure reactions for the 22-nm node and below.

Ultra Low Damage on Photo-resist Patterns

The physical gate length should be less than 20 nm in high-speed devices. As this dimension is much smaller than the limit in current lithography, it is necessary to trim the photo-resist patterns a great deal. Trimmed patterns generally topple over easily or bend because of the lack of adhesion between the photo-resist and underlying materials. Low-speed gas injection and low chamber deposition are utilized to prevent this phenomenon. Fig. 7 shows the results of trimming patterns. Hitachi has excellent 20-nm patterns that were thought to be impossible.

Metal and High-*k* Materials Etch

Low pressure reaction, one of the ECR technology merits, shows excellent advantages in the reaction of low vapor pressure materials, because materials that can be etched at high pressure and high temperature (around 100°C) can be etched at room temperature in the low pressure regime. This tendency has been demonstrated in chemical-reaction simulations and actual experiments. Low temperatures very effectively improve TDDB (time dependent dielectric breakdown).

DIELECTRIC MATERIAL ETCHING APPLICATIONS

Special requirements for all etching-process characteristics are very important in the dry etching

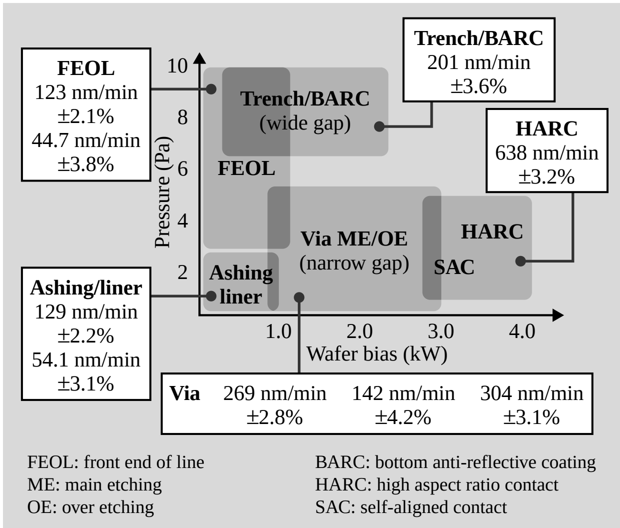

Fig. 8—Process Window for Dielectric Etching with U-8250.
Process-by-process, pressure and wafer bias should be widely changed for Si dielectric etching. U-8250 achieved a wide process window and yielded excellent uniformity.

of dielectric materials in addition to low COO (cost of ownership) and COC (cost of consumables). Hitachi developed a new reactor and a new dry etching system, the U-8250, which can be used over wide pressure and bias-power ranges, as shown in Fig. 8. It features various unique hardware functions and enables highly uniform conditions to be easily and independently set up. Four etching chambers can be installed on the U-8250.

Examples of Damascene Process

High-speed logic manufacturing processes require ten or more sets of Cu DD (dual damascene) levels, based on low-resistive Cu and low-*k* dielectrics. Low COO, contact-hole shrink characteristics, and low damage to porous dielectric materials are a necessity for the via and trench etches of DD. Low COO is achieved by a 4-chamber system and a unique ECP

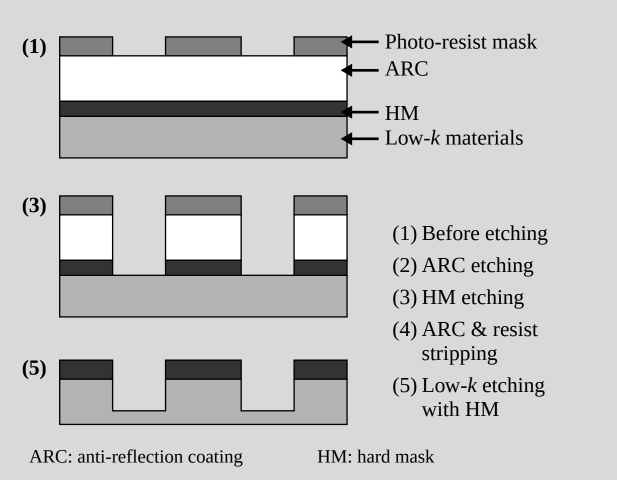

Fig. 9—Dry-etching Flow for Multilayer Mask Process.
A dry-etch flow using a multilayer hard mask process is achieved for Cu metal dual damascene.

(electrically confined plasma) technology, which decreases the deposition of byproducts on the chamber wall during etching and increases the speed at which deposition materials can be removed during cleaning. Other aspects, such as the amount of shrinkage or damage, are minimized by the etch conditions. To date, 25-nm contact hole shrinkage has been demonstrated.

Examples of Metal Hard Mask Etch

It is becoming necessary to study and utilize hard-mask processes as metallization layers and the via and trench feature sizes of the lower damascene layer near the actual device become increasingly smaller and plasma radiation or resist stripping causes critical damage to low-*k* materials. There is an example of the process flow in Fig. 9. In-situ single-chamber etching from (1) to (5) in Fig. 9 is possible due to the wide plasma window of the U-8250. This drastically reduces COO.

Examples of Multilayer Mask Etching

The mask structures for FEOL (front end of line) dry etching became more complex and require hard-mask materials due to the reduced photo-resist thickness and weak resistance to etching of new short-wavelength lithography materials, as shown in Fig. 10. These complex mask structures lead to higher COO. Therefore, high-speed etching of mask layers is required along with excellent etching characteristics. Hitachi developed a new process chemistry that simultaneously achieves etching rates of 300 nm/min, with CD shift of <5.0 nm, and CDU of 3 nm based on the above hardware.

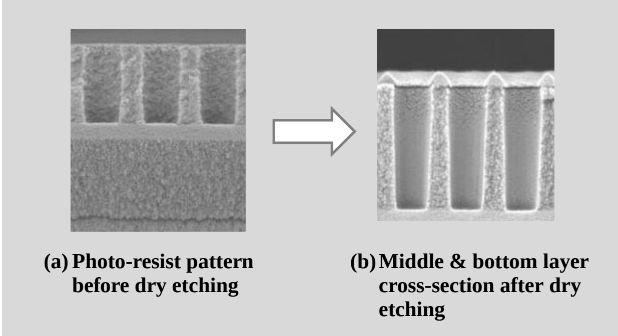

Fig. 10—Examples of Organic Multilayer Mask Etching.
An organic multilayer mask process is widely used for leading edge LSI. Vertical and CD controlled patterns have been achieved.

EXAMPLES OF EQUIPMENT AND PROCESS STABILIZATION

Process Environment Control Technology

PEC (process environment control) can make the treatment environment and process results stable using optimized in-situ cleaning. How effective PEC has been is shown in Fig.11. Time dependent changes in poly-Si etch rates could be reduced from 8% with un-optimized PEC to 3.5% with optimized PEC by OES (optical emission spectroscopy). Further optimizing PEC with EPD (end point detection) could reduce etching rate variations to 1.9%. PEC technology could be combined with process R2R (run to run) control. Time-dependent changes were 1.2% on an experimental basis in this case.

Multi Variate Analysis Technology

MVA (multi variate analysis) is a fundamental technology to achieve AEC/APC. True root causes can quickly be determined from large amounts of data by using MVA. Fig. 12 shows the MVA results between OES intensity and etching specifications such as CD,

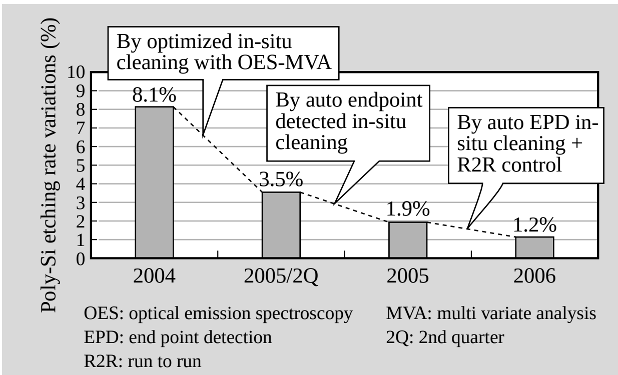

Fig. 11—Decreased Poly-Si Etching Rate Variations by PEC (process environment control).
Variations in the poly Si etch rate can be reduced by optimized in-situ cleaning and R2R control.

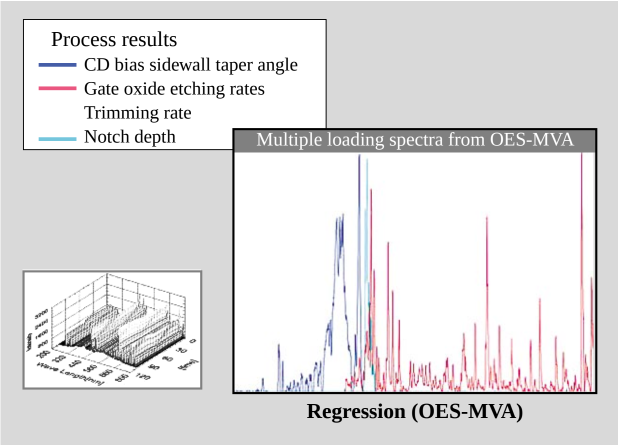

Fig. 12—Analyzed Relationship Between OES Intensity and Etching Characteristics by MVA.
Sensitive emissions to particular etching characteristic could be specified through the MVA of plasma optical emission spectroscopy and etching results.

taper angle, selectivity, amount of notching, and the trimming rate. Quick process setups and etching performance checks are easily executed based on this MVA model.

EPD Technology

Even if the equipment itself is stable, it is possible for wafers to have some variations. EPD was also re-designed to maintain precise control for this reason. Hitachi reduced the minimum detection limit of exposed area to 2% and the detection delay to 0.2 s.

CONCLUSIONS

Excellent dry-etching processes and equipment for 45-nm-node and below semiconductor manufacturing were studied and established by Hitachi.

(1) A simplified and completely symmetrical chamber structure was created.
(2) A gate etching process achieved a CDU of 1.8 nm, an LWR of 3.2 nm, and an I-D bias of 1.0 nm. It also attained trimmed 20-nm-level patterns, and dual metal and high-*k* etching at room temperature.
(3) A dielectric etching chamber that can be used under a wide range of process conditions was created. Low COO DD etching and metal hard mask etching was developed. Etching rates of 300 nm/min etch rates, CD shifts of <5.0 nm, and a CDU of 3 nm were obtained for FEOL multilayer masks.
(4) Various systematic procedures were done to stabilize process. Time-dependent changes could be reduced to 1.2% through active PEC technology.

As Hitachi will continue to develop these procedures for future devices, process characteristics can be further improved over time.

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