Vertical Furnaces for Thin Film Deposition and Annealing Contributing to Low-cost, High-performance Semiconductor Device Manufacturing

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OVERVIEW: Large batch vertical furnaces for thin film formation and annealing play an essential role in modern low-cost, high-performance semiconductor device manufacturing. Working together, Hitachi, Ltd. and Hitachi Kokusai Electric Inc. led the world in the development and commercialization of these vertical furnaces for use in mass production. The vertical furnaces for thin film formation feature nm-order accuracy and can process more than 100 300-mm wafers at a time. The vertical annealing furnaces also feature a high level of accuracy with temperature uniformity of ± 0.5°C. It is anticipated that vertical furnaces will result in further progress in semiconductor manufacturing technology. There is also the potential for the scope of application of vertical furnaces to extend from semiconductor technology into the field of green innovation technologies.

INTRODUCTION

A supply chain able to provide cheap high-performance semiconductor devices as required is a major factor in our advanced information society. Large batch vertical furnaces for thin film formation and annealing are widely used in semiconductor device production. Working together, Hitachi, Ltd. and Hitachi Kokusai Electric Inc. led the world in the development and commercialization of these vertical furnaces for use in mass production. Vertical furnaces in current use are typically able to form thin films on more than 100 300-mm ϕ Si (silicon) wafers at a time with nm-order accuracy and perform annealing with temperature uniformity of ± 0.5°C.

This article describes how vertical furnaces were developed from horizontal furnaces to become mainstream, the latest trends in thin film formation and annealing, and the potential for the scope of application of vertical furnaces to extend from semiconductor technology into the field of green innovation technologies.

BACKGROUND TO DEVELOPMENT OF VERTICAL FURNACES FOR THIN FILM FORMATION AND ANNEALING

History of Horizontal and Vertical Furnaces

Hitachi Kokusai Electric was the first Japanese company to develop furnaces for forming thin films such as SiO_2 (silicon dioxide), SiN (silicon nitride), and poly-Si films on semiconductor devices which it did in the early 1970s. In 1975, it commenced research into a low-pressure CVD (chemical vapor deposition) process that used horizontal furnaces (consisting of heated horizontal quartz reactors and a process gas supply system) and delivered its first machine to Hitachi's Musashi Works in 1976. A plan to "double sales in five years" was formulated in 1984 and set out a strategy of focusing on the development of vertical furnaces. By utilizing the thin film technologies built up through experience with horizontal furnaces and redirecting its approach toward vertical furnaces, the semiconductor equipment business grew steadily. The 1,500th vertical furnace was shipped ten years later in 1994 by which time the product had become the mainstay of the Semiconductor Equipment Division. The 2,000th furnace was supplied to Hitachi, Ltd. in April 1995. This made it unquestionably Hitachi Kokusai Electric's number one product. Further enhancements to the vertical furnaces included automation and load-lock/N_2-purge functions and progress was also made on developing the furnaces to handle larger wafer sizes. Currently, more than 7,000 of Hitachi Kokusai Electric's vertical furnaces are in use around the world where they play a key role in the semiconductor device manufacturing process.

Development of Vertical Furnaces

With the development of technologies for higher levels of integration, the main DRAM (dynamic random access memory) chips produced by the semiconductor industry changed from 64 kbit to 256 kbit around 1983. There was a need to develop equipment able

to handle larger diameter wafers (150-mm diameter) and a smaller design rule (1.3-µm process). Problems that had arisen with conventional horizontal furnaces included intra-wafer and wafer-to-wafer thickness uniformity degradation, the formation of particles and native oxides, and equipment taking up more space because of the need to handle larger wafer diameters. Horizontal furnaces used the "quartz boat transfer in quartz tube with cantilever arm" method to reduce the number of particles. Unfortunately, this method did not eliminate particle formation due to quartz-on-quartz contact. Also, loading a quartz boat into a reactor also allows in a quantity of air resulting in thicker native oxide formation on the wafer surface. Thick native oxides are an obstacle to producing thin oxide films for gate structures. A further problem arose with the strength of the cantilever arm as wafer sizes became larger and the number of wafers per batch grew. To solve these problems, research started on a vertical furnace in which the quartz reaction tube was oriented vertically. Hitachi, Ltd.'s Mechanical Engineering Research Laboratory and the Production Engineering Department of Musashi Works worked together with Hitachi Kokusai Electric on the development which utilized techniques such as thermal simulation and experiments on small-scale models to establish the core technologies for vertical furnaces. Key factors included use of a bottom-opening quartz tube to prevent trapped air, a quartz boat design that prevented contact with the quartz tube, adoption of a four-zone heater and better control of heat generation to achieve superior temperature uniformity, and energy efficiency. The design of the vertical heater used 150 thermocouples embedded in the prototype to optimize the temperature by measuring the actual values and compare them with the simulation results. Reaction simulation was used with the vertical furnace for thin film formation to optimize the equipment and process for large-diameter wafers. The first model was delivered to Hitachi, Ltd. in 1986 (see Fig. 1). Hitachi, Ltd. and Hitachi Kokusai Electric jointly won a technology prize at The Japan Society of Mechanical Engineers' 1992 awards for the successful development of technologies used in the vertical heater[1].

Fig. 1—First Vertical Furnace.
Hitachi, Ltd. and Hitachi Kokusai Electric jointly won a technology award from The Japan Society of Mechanical Engineers in 1992 for their success in developing vertical heater technology.

NEW DEVELOPMENTS FOR VERTICAL FURNACES AND PROCESSES

Serious consideration was first given to the use of high-*k* (permittivity) dielectric films in place of the SiO_2 and SiN films used previously at the start of the 2000s to solve the problem of making dielectric films thinner as smaller design rules were adopted for semiconductor devices. New vertical furnaces and processes were developed for thin film formation to achieve better film thickness uniformity and more accurate composition control than the conventional low-pressure CVD process. Hitachi Kokusai Electric undertook a study of high-*k* dielectric films in collaboration with Hitachi, Ltd. Mechanical Engineering Research Laboratory in 2001 to 2003 to clarify how to proceed with development. It went on to develop vertical furnaces and processes for metal films as well as low-temperature SiO_2, SiN, and other films resulting in a low-temperature film formation process with better film thickness uniformity than was possible using the conventional low-pressure CVD process.

The early 2000s also brought demand for using vertical furnaces for epitaxial growth with high productivity and Hitachi Kokusai Electric sought the assistance of Tohoku University and Hitachi Research Laboratory to develop a load-lock system with a level of cleanliness that was significantly better than previous methods. This was the first time low-temperature epitaxial growth had ever been achieved in a vertical furnace[2].

In the case of vertical furnaces used for oxidation,

Hitachi Kokusai Electric has improved on the conventional wet oxidation process to develop a new oxidation process that achieves a uniform oxide film from the surface to the bottom of the deep trench and which minimizes crystal orientation dependency in the Si substrate. Potential applications include three-dimensional transistors for advanced logic devices and memory-cell-selection transistors for DRAM.

As well as contributing to business growth at Hitachi Kokusai Electric, these new vertical furnaces[3] are helping re-establish a place for vertical furnaces in advanced device development where use of single-wafer processing equipment has become standard practice. The following section describes some detailed examples of this technology.

TECHNOLOGY TRENDS FOR VERTICAL FURNACES

Technology Trends for Vertical Furnaces Used for Thin Film Formation

The achievement of high performance and a high level of integration in the production of advanced semiconductor devices requires techniques for forming high-quality dielectric films at even lower temperatures and even finer structures with superior step coverage. High-productivity processes are also essential for supplying devices at lower cost. To overcome these challenges, Hitachi Kokusai Electric has established a process for forming dielectric films with good step coverage, relatively low process temperature, and high film quality by developing the new film formation techniques described earlier. It is anticipated that this technology will solve many of the challenges facing the next generation of memory and logic devices.

In addition to using the new film formation process to adopt dielectric films for transistor gate side-wall spacers and in DRAM capacitors, other work in progress includes investigation of sacrificial films and how to overcome the limits that the resolution of the photo lithography process imposes on pattern formation. At Hitachi Kokusai Electric, technology for smaller design rules is called “SRP (super resolution patterning) technology” and the company supplies equipment and processes that allow precise control of film thickness. Hitachi Kokusai Electric has also developed processes for film formation at very low temperatures that allow films to be formed on materials such as photo resist and amorphous carbon that are not compatible with previous techniques.

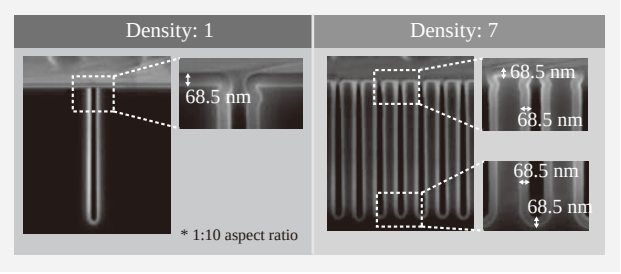

Fig. 2—Good Step Coverage.
A nanometer level of film thickness control was achieved by using a new film formation technique.

Another problem associated with lowering the film formation temperature is the difficulty of achieving the wet-etching immunity required in the process. To solve this problem, Hitachi Kokusai Electric developed a low-wet-etching-rate film.

The new film formation technique has excellent characteristics which include precise film thickness control, low-temperature film formation, good step coverage, and freedom from loading effects (pattern dependence). Fig. 2 shows cross-sections of high-quality SiO_2 films formed using the new technique on Si substrate samples with a deep trench (1:10 aspect ratio) and different surface densities. The thicknesses at surface, trench side wall, and trench bottom of the substrate of density 7 and at the surface of the substrate of density 1 are all 68.5 nm, demonstrating that nm-order accuracy thin film formation is achieved regardless of factors such as the trench and its density.

When first developed, the new technology had a problem with inferior productivity. To achieve a major improvement in productivity, a new material supply mechanism, reaction chamber, and ventilation system were developed utilizing computational fluid dynamics. The following describes each development in detail.

(1) Material supply mechanism

The ability to quickly and accurately raise the partial pressure of source gases is important when supplying materials to the wafer surface. To achieve this, Hitachi Kokusai Electric shortened the material supply time by adopting a mechanism able to supply materials to the reaction chamber quickly and with high precision.

A growing number of film materials including high-*k* films such as Al_2O_3 or HfO_2 are liquids at room temperature and atmospheric pressure. Because these materials have a low vapor pressure and are prone to thermal decomposition, particles can easily be produced. Consequently, to achieve reliable gasification in the supply mechanism without the

Fig. 3—QUIXACE Vertical Annealing Furnace for 300-mm Wafers.
The furnace supports applications ranging from temperatures as low as 150°C up to a very high 1,350°C.

materials thermally decomposing, a uniform heating method was implemented with optimum conductance by using computational fluid dynamics to design a material supply mechanism.

(2) Reactor with plasma source

Si and N (nitrogen) are included in the process gas for SiN film formation. When film formation takes place in the sub-600°C temperature range, it is necessary for the activated species of the N process gas to be generated in very close proximity to the wafer. Hitachi Kokusai Electric devised a mechanism that was the first in the world to use a plasma source in the reaction chamber of a vertical furnace to achieve effective generation of the activated species of N process gas. This also significantly reduced the time taken to supply the N process gas compared to previous systems that used an external plasma source.

(3) Ventilation system

A new type of ventilation system was adopted for some of the new film formation processes. This improved productivity by allowing the maintenance cycle associated with the accumulation of deposited material to be extended and the purge time to be shortened.

Technology Trends for Vertical Annealing Furnaces

The Hitachi Kokusai Electric vertical annealing furnace shown in Fig. 3 was developed for use by wafer manufacturers and has a dominant market share. The following sections describe the demand for annealing furnaces, the market requirements, and the features of Hitachi Kokusai Electric's equipment and technologies.

(1) Demand for high-temperature annealing furnaces

High-temperature annealing furnaces are used by wafer manufacturers in the production of annealed wafers and SOI (Si-on-insulator) wafers. Currently, however, the market for these machines is undergoing a sharp contraction due to the recent shrinking of the market for annealed wafers and lack of growth in the use of SOI wafers. Instead, demand from manufacturers is growing for other types of annealing such as STI (shallow trench isolation) annealing and machines for this purpose now make up the bulk of sales.

(2) Market requirements for annealing furnaces

As in the past, the key requirements in high-temperature annealing are for slip-free processing, elimination of underside defects, a high level of cleanliness, and high throughput.

(3) Hitachi Kokusai Electric's vertical annealing furnaces

Hitachi Kokusai Electric's annealing furnaces feature a heater with a longer uniform-temperature region (±0.5°C, 1,150 mm) than competing products and the ability to handle 100 wafers per batch for 1,200°C annealing. They also incorporate a high-speed wafer transport mechanism to support high-throughput processing. The furnace is available with a range of different heaters giving it an operating range from low (150°C) to very high temperatures (1,350°C). For operation at very high temperatures, slip-free processing is achieved by supporting the wafers on a unique board-shaped fitting to minimize intra-wafer stress. Fig. 4 shows an X-ray topography photograph

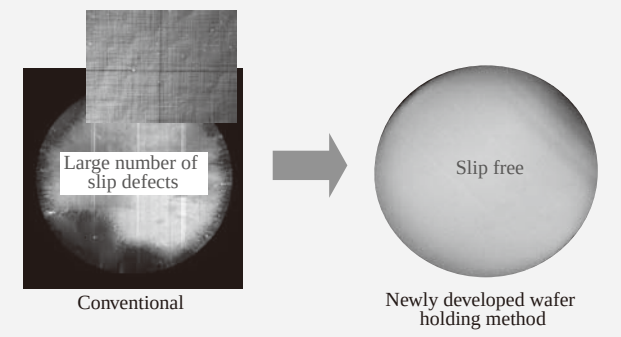

Fig. 4—X-ray Topography Photograph after 1,350°C Annealing Process.
The very-high-temperature annealing process achieves high throughput of large 300-mm wafers while minimizing the slip that occurs in the high-temperature (1,350°C) process.

of a Si substrate annealed at 1,350°C. Whereas slip defects occur all over the surface of the wafer processed using the conventional wafer holding method, no slip defects are evident when the newly developed wafer holding method is used.

FUTURE OUTLOOK FOR VERTICAL FURNACES

Even as semiconductor device manufacturing processes become smaller, more complex, and cheaper, vertical furnaces are likely to continue to play an important role. For example, some leading device manufacturers have already started pilot lines using wafers with a diameter of 450 mm with the aim of reducing costs further. Vertical furnaces will remain essential even if 450-mm wafers are adopted for the oxidation and annealing processes. Although numerous challenges remain to be overcome, including how to make equipment take up less space, problems with greater intra-wafer temperature variation as the heater heats up and cools down, and temperature uniformity at steady-state, Hitachi Kokusai Electric believes it can solve these problems by applying new technologies and drawing on its past experience in moving to larger wafer diameters.

In addition to supporting 450-mm ϕ wafers, it is anticipated that vertical furnaces will also be able to be used in new applications other than Si wafer processing. Use in the SiC wafer process is one such example. SiC is a promising candidate for use in energy-efficient power devices and its production process requires epitaxial growth furnaces and annealing furnaces for mass production that can operate at very high temperatures (up to 1,600°C and 1,800°C respectively). Using vertical furnaces to achieve this is highly desirable. This process involves temperatures outside the range used in Si device production and the development of vertical furnaces equipped with new heating systems able to generate very high temperatures in place of the resistance heating used in the past will likely make the introduction of full-scale SiC device production easier and help accelerate green innovation.

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